IATEC

IGEP™ TECHNOLOGY

IGEP™ SMARC iMX6

HARDWARE REFERENCE

SMARC module

SGeT STANDARDIZATION GROUP FOR EMBEDDED TECHNOLOGIES

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Revision	Date	Description
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1.1	03/02/2016	• First Review
1.2	03/10/2016	• SMARC Table Review
1.3	04/23/2016	• Design Changes
2.0	04/06/2021	• Second Review

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2 INTRODUCTION

2.1 PRODUCT DESCRIPTION

The IGEP™ SMARC iMX6 is an industrial low computer module based on ARM Cortex-A9 at speeds up to 1.2 GHz by NXP iMX6 family of processors.

It is an industrial computer module (it can work in a temperature range from -40ºC to +85ºC), in a very low profile according the standard form factor SMARC by SGET (its size is only 82,00 mm x 50,00 mm). With different combinations of RAM and Flash memory (see customized possibilities at chapter 2.4) and a complete list of interfaces and peripherals including 3D graphic accelerator, it can be the base for a complex industrial equipment or any other kind of application.

For development purposes there is also available an expansion board (IGEP™ SMARC EXPANSION) to complete the module. It can be used as the fastest way to develop the user's final application before the prototyping phase. This expansion board can be used with all IGEP™ SMARC modules.

Highlights:

- Fully tested, highly reliable, scalable, efficient and high performing board that allows customers to focus on their end application.
- Designed for industrial range purposes (temperature range: -40 ºC to +85 ºC).
- Form factor according to small size SMARC (82,00 mm x 50,00 mm).
- Easy connectivity through MXM3 graphic cards type connector: 314-pin, 0,5 pitch right angle.
- 1V8 I/O level signals.
- JTAG interface available.
- Based on NXP iMX6 processor which has an advanced ARM Cortex-A9 core.
- The iMX6 Family processors are based on the enhanced device architecture and include the NEON™ Media coprocessor.
- One available 10/100/1000 Mbps Ethernet MAC+PHY interface.
- WiFi 802.11 b/g/n / Bluetooth 4.2 connectivity
- RAM memory size: Up to 2 GB.
- Flash memory size: Up to 8 GB eMMC.
- Low Power solution.
- Compatible with SMARC modules.

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2.2 IGEP™ SMARC iMX6 BENEFITS AND APPLICATIONS

There are a lot of advantages that developers will find in the IGEP™ SMARC iMX6 series. Reducing the implementation time and saving costs on their designs. Amongst others, the main benefits are the following:

- Easy scalability between different modules (even with other processors) thanks to the SMARC standard.
- Compact and powerful core for new products.
- Robust and easy to mount due to the MXM3 314-pin connector.
- Reduced time to market.
- Low power consumption ≤ 2W.
- Industrial Temperature Range -40 to +85ºC.
- Extended life range product.

At the same time, it can be implemented in all kind of end applications. The followings are just a few ones, but the list can be as long as the imagination of the developers.

- Connected vending machines.
- Home / Building automation (IoT applications).
- Human Interface.
- Industrial Control.
- Test and Measurement.
- Artificial Intelligence

2.3 SMARC STANDARD

The IGEP™ SMARC iMX6 accomplish the SMARC 1.1 standard with some components of SMARC 2.0 version, which is defined by SGET.

The SMARC (“Smart Mobility Architecture”) is a computer Module definition targeting applications that require low power, low costs, and high performance. This standard is based on the former ULP-COM standard (Ultra Low Power Computer-on-Modules). The Modules will typically use ARM SoCs (System on Chip) families or similar.

SMARC standard defines two module sizes (82mm x 50mm and 82mm x 80mm). **All the available IGEP modules sizes 82mm x 50mm**. The Module PCBs have 314 edge fingers that mate with a low profile 314 pin (156 on TOP side and 158 on BOTTOM side) right angle connector. The module pins are designated as P1-P156 on the TOP side and S1 – S158 on the BOTTOM side. The connector is sometimes identified as a 321-pin connector, but 7 pins are lost to the key (4 on the TOP side and 3 on the BOTTOM side).

The Modules are used as building blocks for portable and stationary embedded systems. The core CPU and support circuits, including DRAM, boot flash, power sequencing, CPU power supplies, GBE and a single channel LVDS display transmitter are concentrated on the Module. The modular approach allows scalability, fast time to market and upgradability while still maintaining low costs, low power and small physical size.

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2.4 SMARC FORM FACTOR FEATURE SUMMARY

Small form factor, low profile and low power edge-finger card format Module with pin-out optimized for ARM and x86 architecture processors; may also be used with low power, tablet oriented X86 and RISC devices.

- Two Module sizes:
  - 82mm x 50mm.
  - 82mm x 80mm.
- Carrier Board connector: 314 pin 0.5mm pitch R/A memory socket style connector
  - Originally defined for use with MXM3 graphics cards.
  - SMARC Module pin-out is separate from and not related to MXM3 pin-out.
  - Multiple sources for Carrier Board connector.
  - Low cost.
  - Low profile:
    - As low as 1.5mm (Carrier Board top to Module bottom).
    - Other stack height options available, including 2.7mm, 5mm, 8mm.
    - Overall assembly height (Carrier Board top to tallest Module component) is less than 6mm.
  - Excellent signal integrity – suitable for 2.5 GHz / 5 GHz / 8 GHz data rate signals such as PCIe Gen 1, Gen 2 and Gen 3.
  - Robust, vibration resistant connector.
- Module input voltage range: 3.0V to 5.25V
  - Allows operation from 3.6V nominal Lithium-ion battery packs.
  - Allows operation from 3.3V fixed DC supply.
  - Allows operation from 5.0V fixed DC supply.
  - Single supply (no separate standby voltage).
  - Module power pins allow 5A max.
- Low power designs
  - Fanless.
  - Passive cooling.
  - Low standby power.
  - Design for battery operation.
  - 1.8V default I/O voltage.

2.5 IGEP™ SMARC iMX6 SERIES

The IGEP™ SMARC iMX6 series is composed by different models, all of them have the same general circuit but they change in the CPU, the RAM memory, the storage memory and the connectivity used.

In next chapter 2.6 are commented the main differences according to all models.

Other combinations are available. Contact with IATEC's Sales Department for other configurations.

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2.6 PARTS NUMBERS

Depending on the module configuration, the module has different parts numbers.

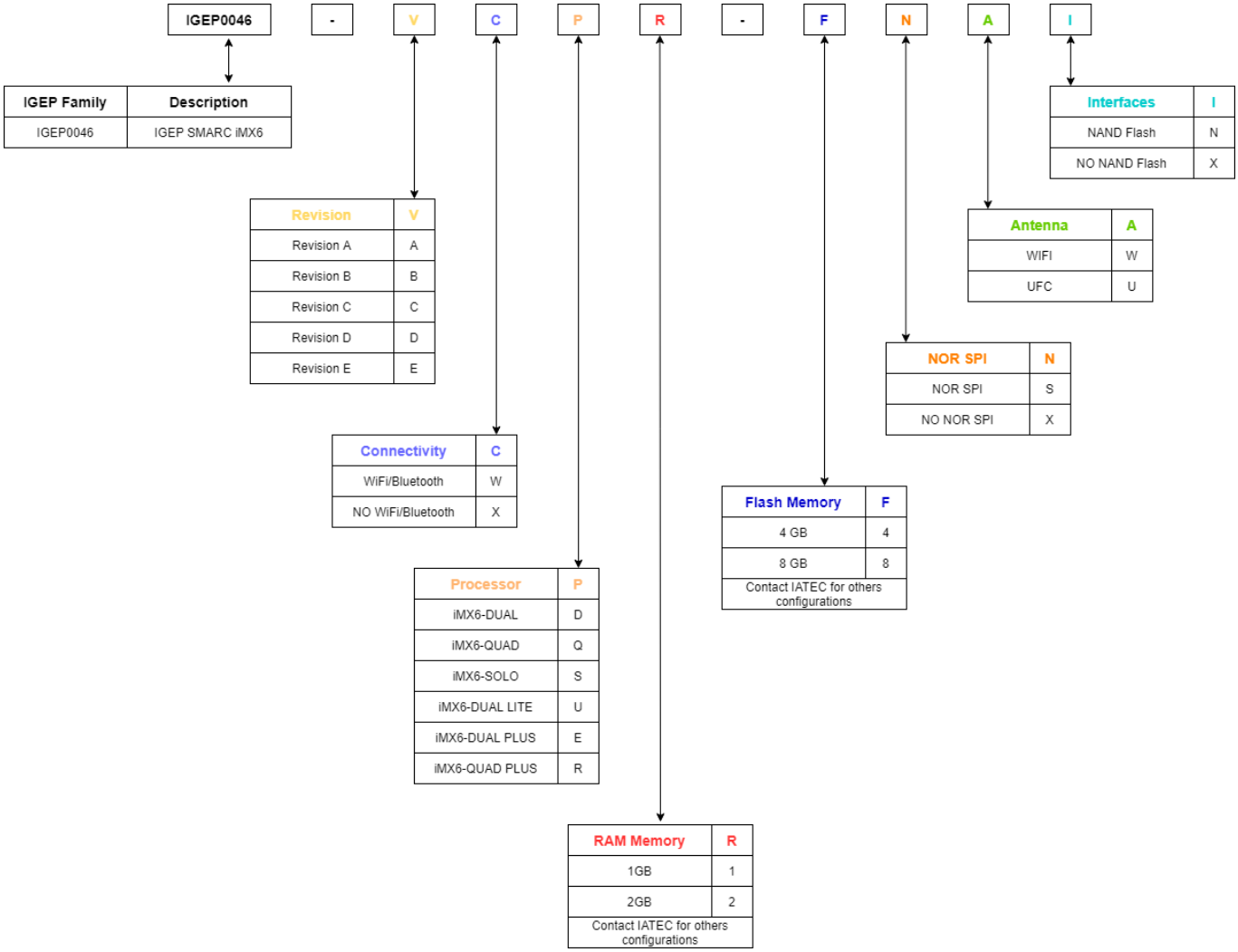

Figure 1 IGEP™ SMARC iMX6 Possible Part Number

Part Number	IGEP™ Device	Description
IGEP0046-EWD2-8SXX	SMARC iMX6-DUAL WiFi	Processor: iMX6 DUAL RAM Memory: 2 GB Flash Memory: 8 GB Connectivity: WiFi 802.11 b/g/n / Bluetooth 4.2 NOR SPI
IGEP0046-EWQ1-8SXX	SMARC iMX6-QUAD WiFi	Processor: iMX6 QUAD RAM Memory: 1 GB Flash Memory: 8 GB Connectivity: WiFi 802.11 b/g/n / Bluetooth 4.2 NOR SPI

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IGEP0046-EWQ2-8SXX	SMARC iMX6-QUAD WiFi	Processor: iMX6 QUAD RAM Memory: 2 GB Flash Memory: 8 GB Connectivity: WiFi 802.11 b/g/n / Bluetooth 4.2 NOR SPI
IGEP0046-EWS2-8SXX	SMARC iMX6-SOLO WiFi	Processor: iMX6 SOLO RAM Memory: 2 GB Flash Memory: 8 GB Connectivity: WiFi 802.11 b/g/n / Bluetooth 4.2 NOR SPI
IGEP0046-EWU1-4XXX	SMARC iMX6-DUAL LITE WiFi	Processor: iMX6 DUAL LITE RAM Memory: 1 GB Flash Memory: 4 GB Connectivity: WiFi 802.11 b/g/n / Bluetooth 4.2
IGEP0046-EWU1-4XUX	SMARC iMX6-DUAL LITE WiFi	Processor: iMX6 DUAL LITE RAM Memory: 2 GB Flash Memory: 8 GB Variant without WIFI antenna but UFL connector
IGEP0046-EWU2-4XXX	SMARC iMX6-DUAL LITE WiFi	Processor: iMX6 DUAL LITE RAM Memory: 2 GB Flash Memory: 4 GB Connectivity: WiFi 802.11 b/g/n / Bluetooth 4.2
IGEP0046-EWU2-4XXX	SMARC iMX6-DUAL LITE NO WiFi	Processor: iMX6 DUAL LITE RAM Memory: 2 GB Flash Memory: 4 GB
IGEP0046-EWU2-8XXX	SMARC iMX6-DUAL LITE NO WiFi	Processor: iMX6 DUAL LITE RAM Memory: 2 GB Flash Memory: 8 GB
IGEP0046-EWE2-8SXX	SMARC iMX6-DUAL PLUS WiFi	Processor: iMX6-DUAL PLUS RAM Memory: 2 GB Flash Memory: 8 GB Connectivity: WiFi 802.11 b/g/n / Bluetooth 4.2 NOR SPI

Table 1 IGEP™ SMARC iMX6 Ordering Information.

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3 HARWARE OVERVIEW

3.1 IGEP™ SMARC iMX6

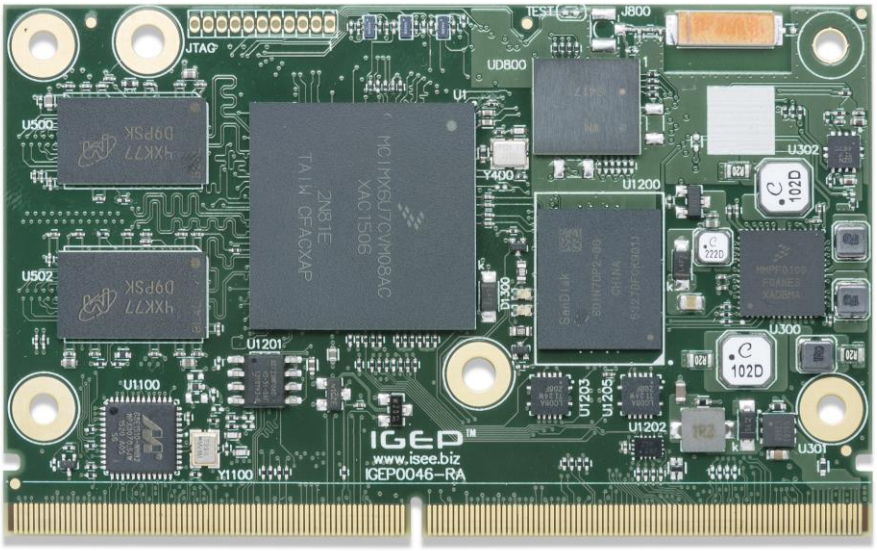

Figure 2 SMARC iMX6 – Top View

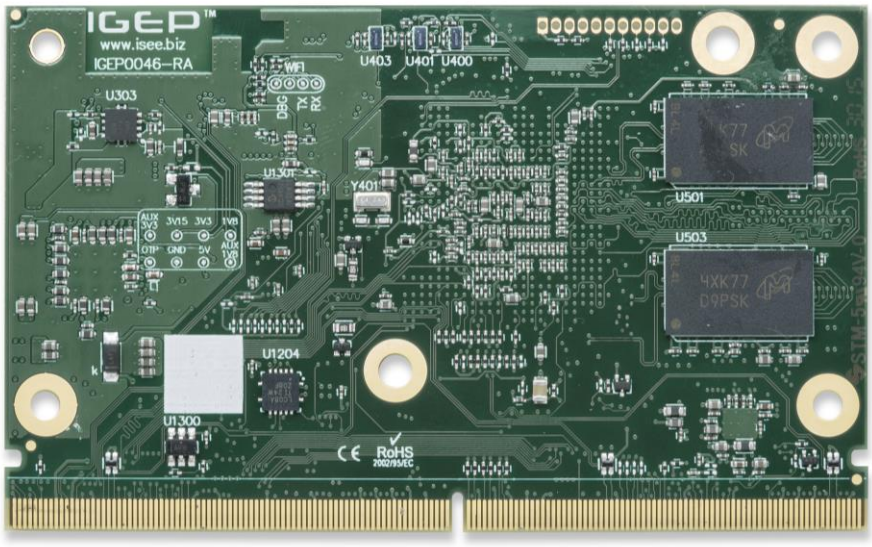

Figure 3 SMARC iMX6 – Bottom View

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3.2 IGEP™ SMARC iMX6 BLOCK DIAGRAM

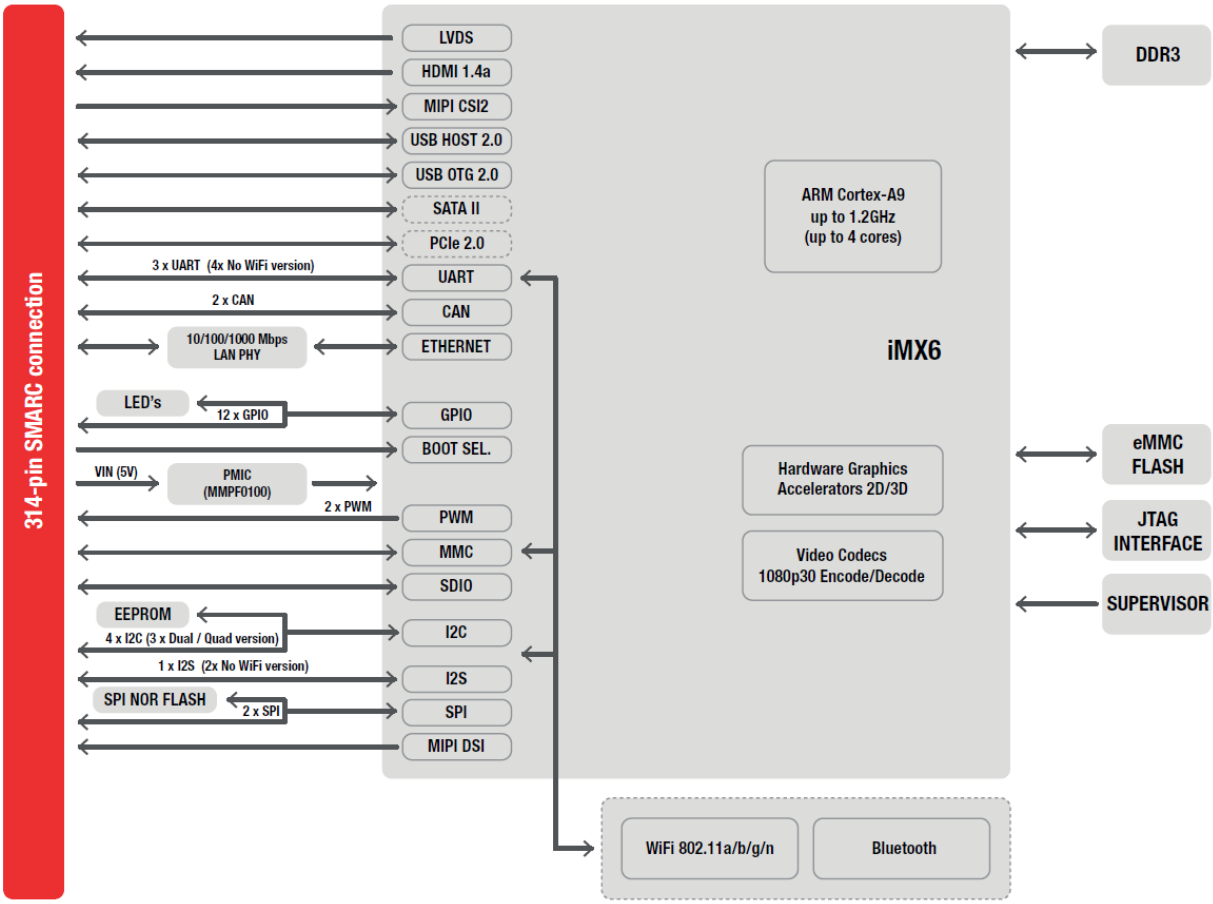

Figure 4 IGEP™ SMARC iMX6 Block Diagram

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3.3 IGEP™ SMARC iMX6 FEATURES

Feature	Specifications
Processor	NXP iMX6 CPU: ARM Cortex-A9 NEON SIMD Coprocessor Frequency: 1.2 GHz (1 GHz in SOLO and DUAL LITE versions)
Memory	RAM: Up to 2 GB DDR3 Flash: Up to 8 GB eMMC
Camera Interface	1 x Parallel Camera 20-bit and 148.5MHz pixel clock Support BT.656 interface
Display	2 x 24-bit Parallel RGB up to WXGA (1366x768) at 60 Hz Support: 24-bit, 18-bit, 16-bit and 8-bit parallel display
Digital Audio	1 x I2S(SAI) (No WiFi versions: 2x)
Network	One Ethernet: 10/100/1000 Mbps WiFi: Certified 802.11 b/g/n (Access Point: Yes) Bluetooth: 4.2
Antenna	Internal WiFi/Bluetooth antenna Optional: U.FL connector for external antenna
USB	1 x USB 2.0 OTG (with integrated phy) 1 x USB 2.0 Host (with integrated phy)
External Interfaces	3 x UART (No WiFi versions: 4x) 4 x I2C 1 x HDMI 2 x SPI 2 x CAN 12 x GPIO 1 x JTAG 1 x EEPROM
OS Support	Linux Kernel 4.9 Distributions: Ubuntu 16.04, Yocto 2.3, Debian
Power Supply	Power from expansion connectors: From 3.0 V to 5,25 V Digital I/O voltage: 1,8 V
Power Consumption	0.32 A
Thermal	Industrial temperature: -40ºC to +80ºC
Form Factor	Small SMARC size: 82,00 mm x 50,00 mm
Humidity	93% relative Humidity at 40 ºC, non-condensing (according to IEC 60068-2-78)
MTBF	131400 hours (>15 years)

Table 2 On-board features

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3.4 IGEP™ SMARC iMX6 COMPONENTS MAP

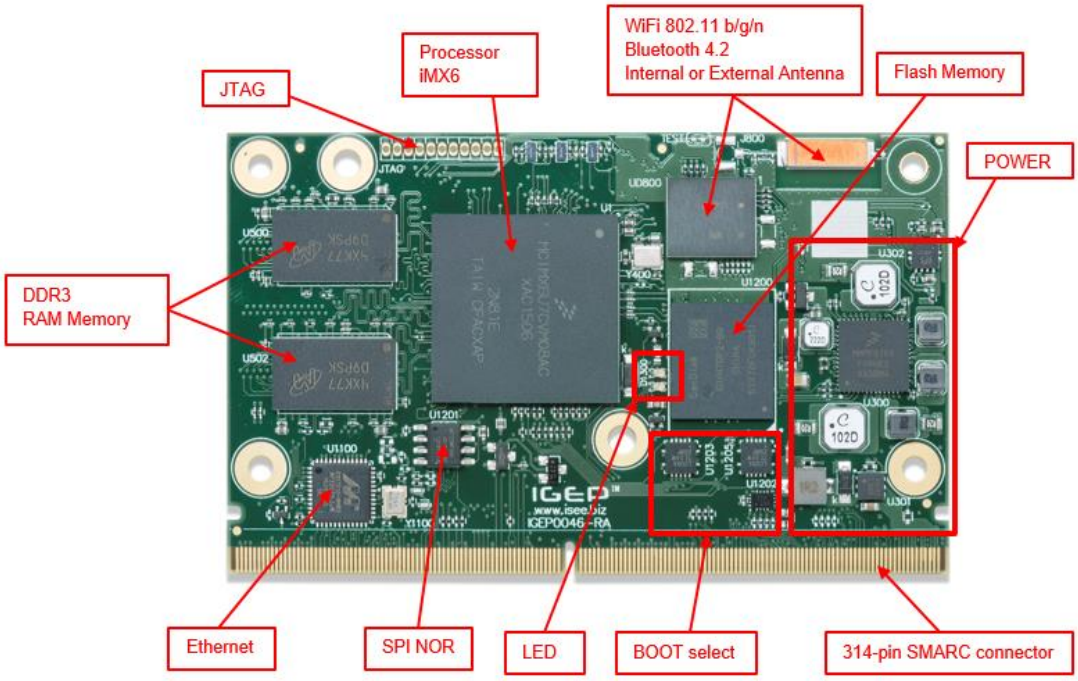

Figure 5 SMARC iMX6 Components Map

3.5 NXP iMX6 PROCESSORS

The iMX6-DUAL by NXP is a highly integrated processor based on two ARM Cortex-A9 with a frequency speed of 1.2 GHz (Industrial version).

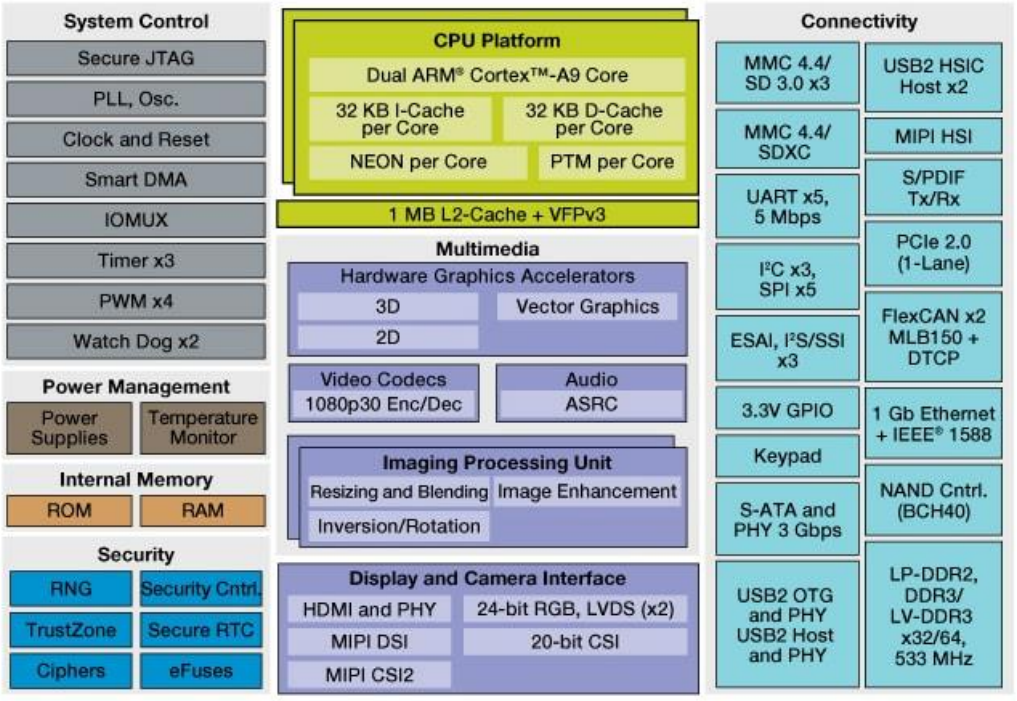

Figure 6 NXP iMX6-DUAL Processors Block Diagram

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The iMX6-QUAD by NXP is a highly integrated processor based on four ARM Cortex-A9 with a frequency speed of 1.2 GHz (Industrial version).

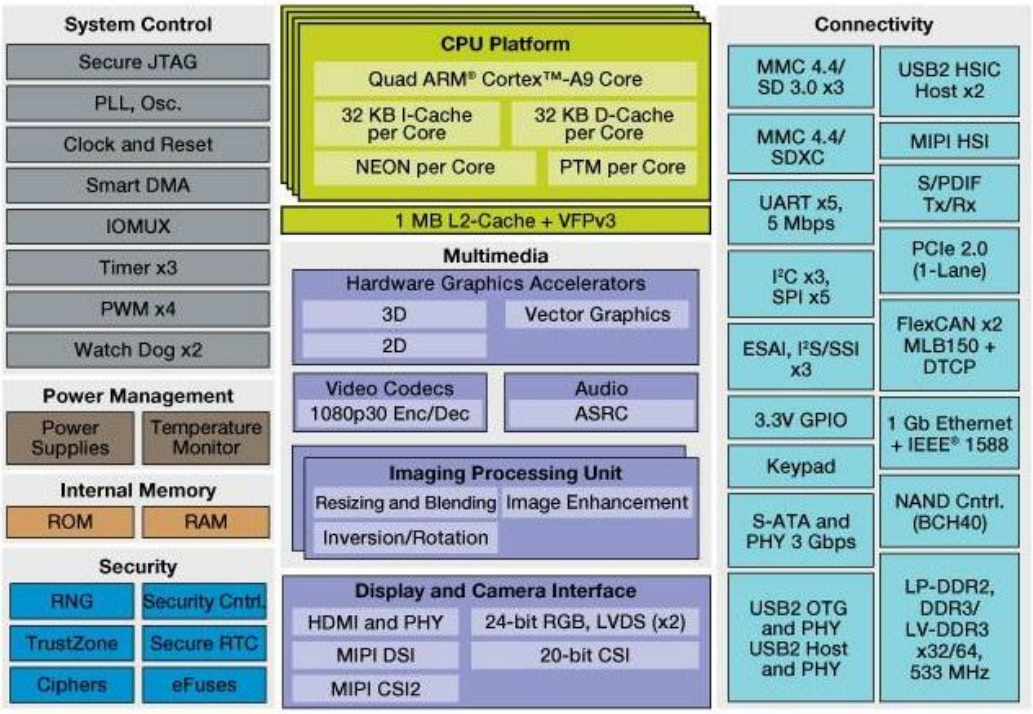

Figure 7 NXP iMX6-QUAD Processors Block Diagram

The iMX6-SOLO by NXP is a highly integrated processor based on one ARM Cortex-A9 with a frequency speed of 1 GHz (Industrial version).

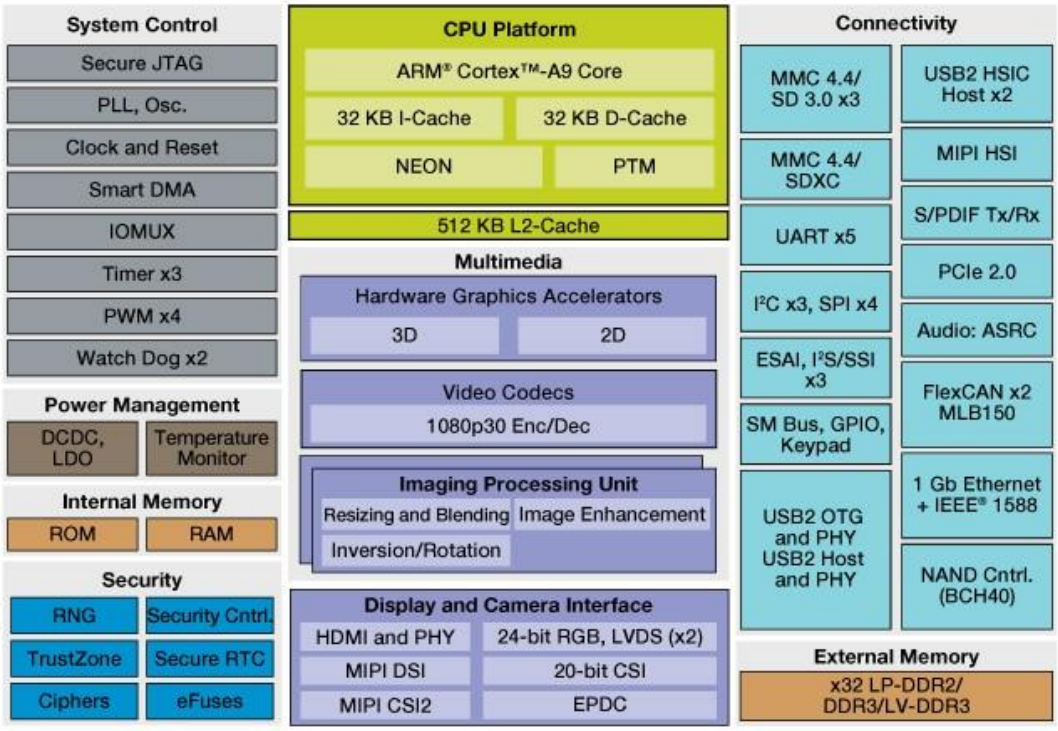

Figure 8 NXP iMX6-SOLO Processors Block Diagram

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The iMX6-DUAL LITE by NXP is a highly integrated processor based on two ARM Cortex-A9 with a frequency speed of 1 GHz (Industrial version).

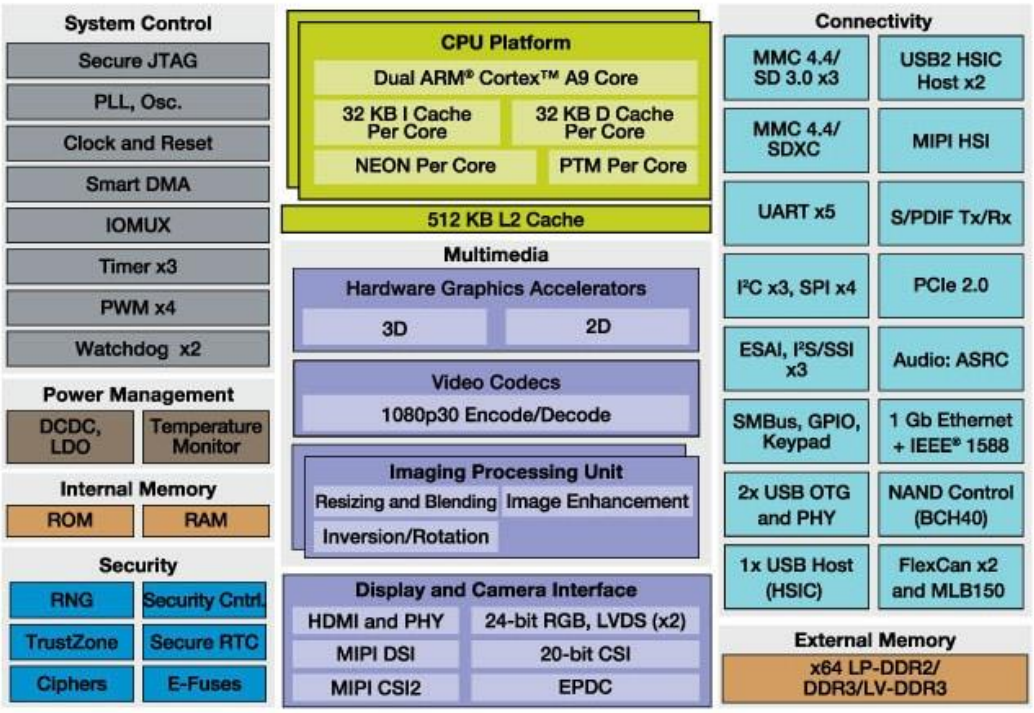

Figure 9 NXP iMX6-DUAL LITE Processors Block Diagram

The iMX6-DUAL PLUS by NXP is a highly integrated processor based on two ARM Cortex-A9 with a frequency speed of 1.2 GHz (Industrial version).

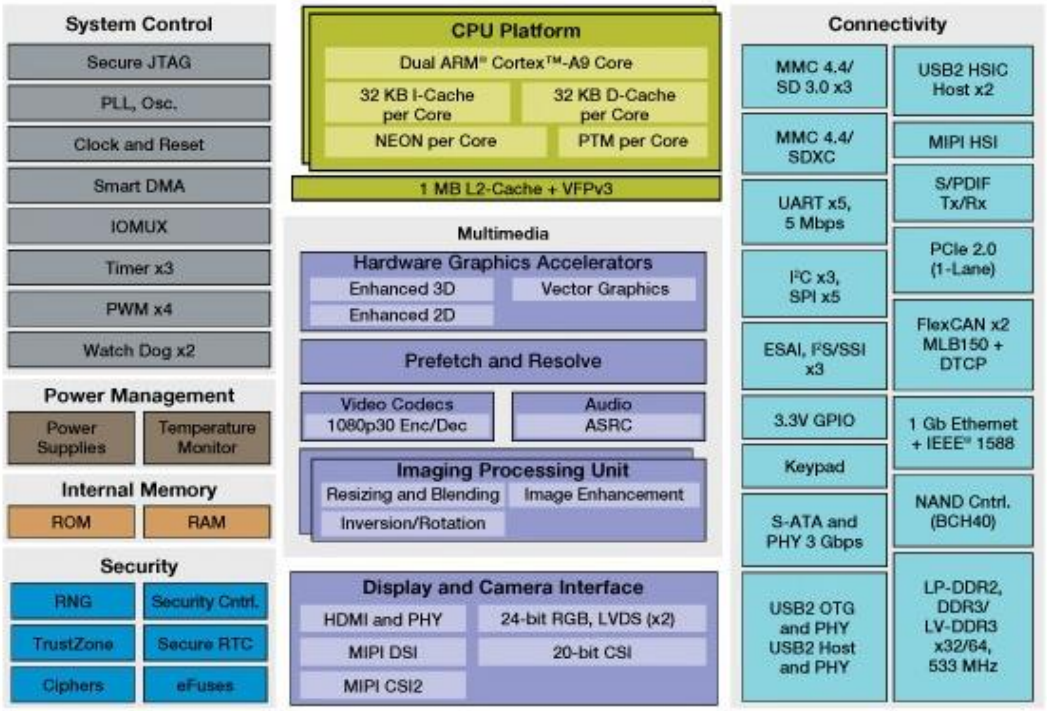

Figure 10 NXP iMX6-DUAL PLUS Processors Block Diagram

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The iMX6-QUAD PLUS by NXP is a highly integrated processor based on four ARM Cortex-A9 with a frequency speed of 1.2 GHz (Industrial version).

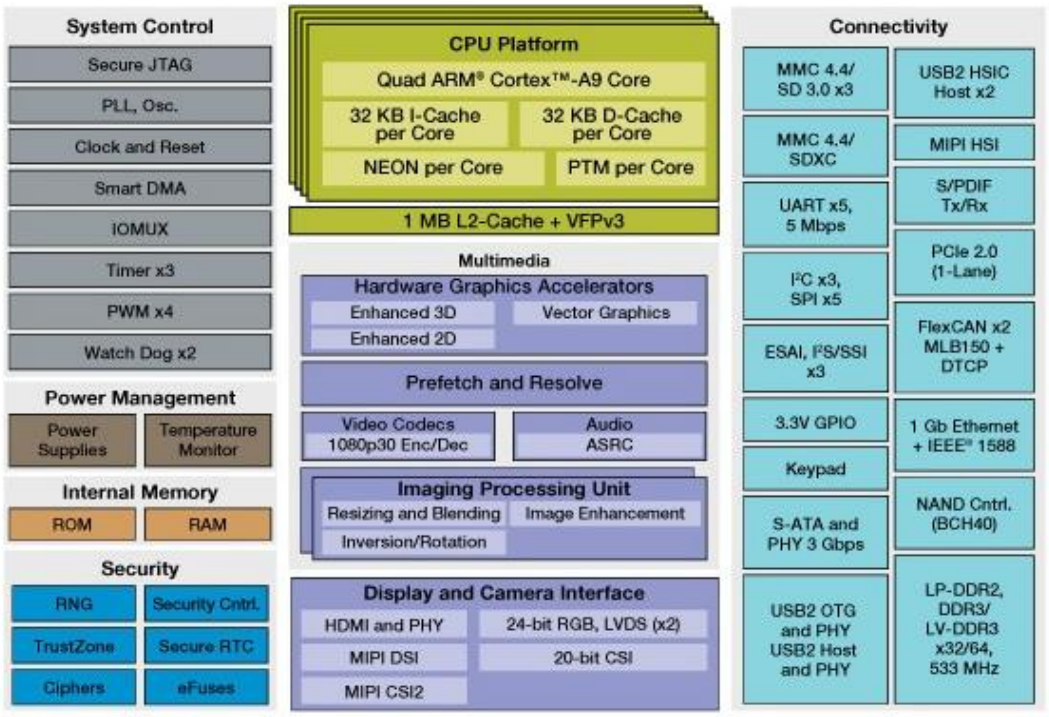

Figure 11 NXP iMX6-QUAD PLUS Processors Block Diagram

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4 SMARC EXPANSION CONNECTOR INTERFACE

4.1 SMARC INTERFACE DEFINITION

IGEP™ SMARC iMX6 has a 314-pin SMARC interface (156 on TOP side and 158 on BOTTOM side), providing source power and 1V8 CMOS signals to support lots of iMX6 processor features which could be used in custom application. The module sizes are 82mm x 50mm as the SMARC standard defines.

Next figure shows the area and pin numbering of the SMARC interface.

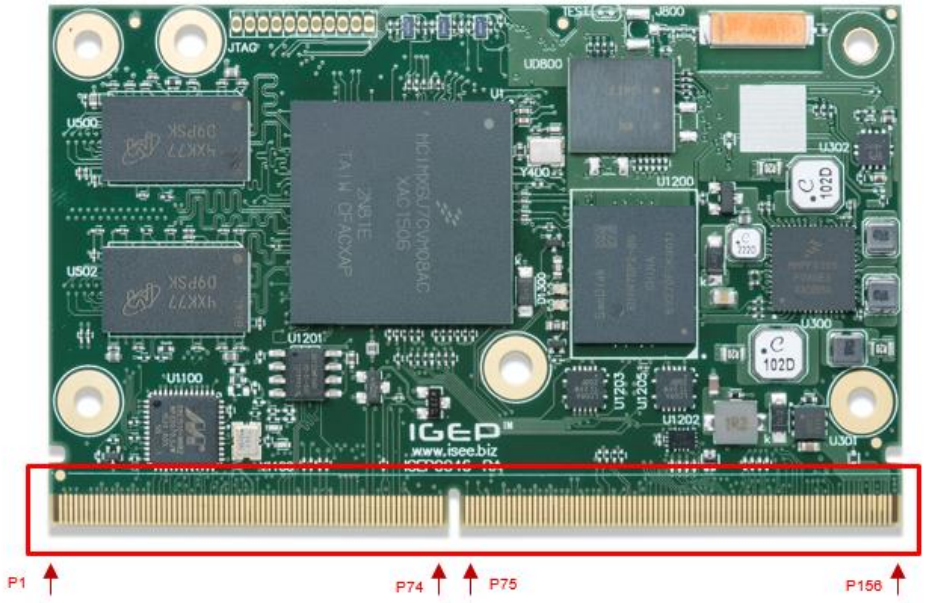

Figure 12 SMARC interface area (TOP Side)

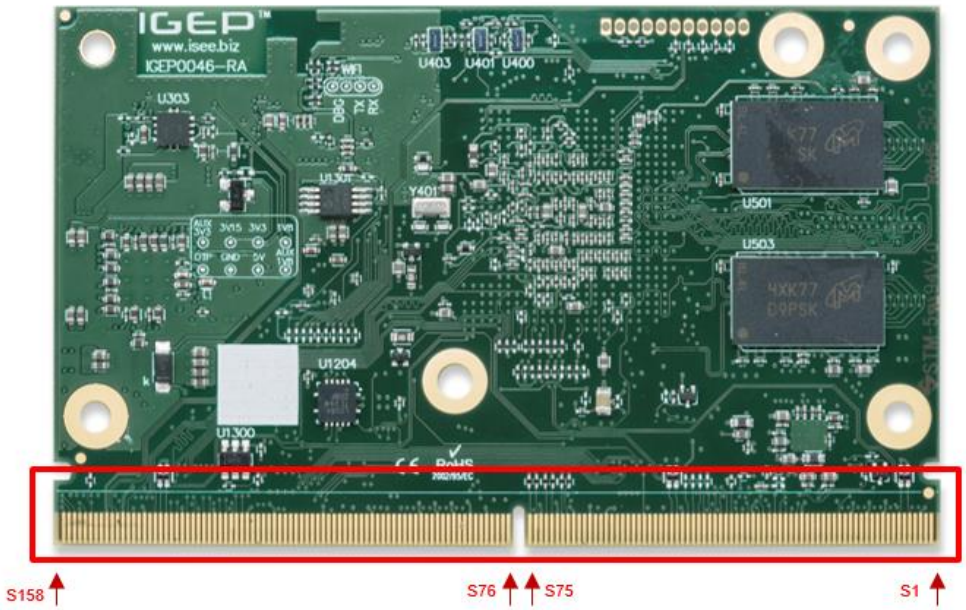

Figure 13 SMARC interface area (BOTTOM Side)

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The IGEP™ SMARC iMX6 modules can be inserted like a target through this SMARC interface to any of the standard connectors existing on the market. Next table shows some valid references (consult the page 73 on the SMARC 2.1 Specification to find more information).

Manufacturer	Part Number	Height
FOXCONN	AS0B821-S43B-*H	4,3 mm
FOXCONN	AS0B821-S43N-*H	4,3 mm
FOXCONN	AS0B826-S43B-*H	4,3 mm
FOXCONN	AS0B826-S43N-*H	4,3 mm
JAE	MM70-314B2-1-R500	4,3 mm
Aces	91781-314 2 8-001	5,2 mm
FOXCONN	AS0B821-S55B-*H	5,50 mm
FOXCONN	AS0B821-S55N-*H	5,50 mm
FOXCONN	AS0B826-S55B-*H	5,50 mm
FOXCONN	AS0B826-S55B-*H	5,50 mm
FOXCONN	AS0B821-S78B-*H	7,80 mm
FOXCONN	AS0B821-S78N-*H	7,80 mm
FOXCONN	AS0B826-S78B-*H	7,80 mm
FOXCONN	AS0B826-S78N-*H	7,80 mm
Yamaichi	CN113-314-2001	7,80 mm

Table 3 Valid SMARC connector part numbers

Developers must consider the SMARC connector height according to their expansion board needs.

Note: Many of the vendor drawings for the connectors listed above show a PCB footprint pattern for use with an MXM3 graphics card. This footprint, and the associated pin numbering, is not suitable for SMARC use. The MXM3 standard gangs large groups of pins together to provide ~80W capable power paths needed for X86 graphics cards.

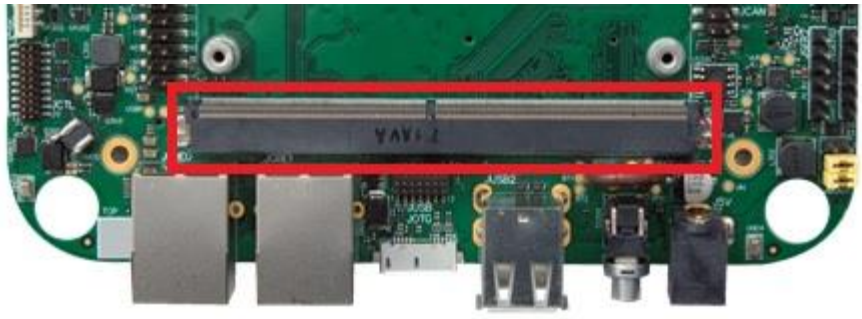

Figure 14 SMARC CONNECTOR

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4.2 PINOUT TABLE OF SMARC (VERSION) EXPANSION INTERFACE

This chapter contains all the pinout details for the SMARC-314 expansion interface. The tables below show the meaning of each column in table 6, where is collected all the pins and its main functions.

COLUMN	INFORMATION PROVIDED	
PIN	Indicates the pin number of the SMARC-314 interface. It is either for Primary Side (Top Side, P#) and Secondary Side (Bottom Side, S#)	
VOLTAGE LEVEL	Signal Level Voltage	
	5V	5 V signal
	3V3	3,3 V signal
	1V8	1,8 V signal
	DS	Differential analog signaling.
	GBE MDI	Differential analog signaling for Gigabit Media Dependent Interface.
	PHY MDI	Differential analog signaling for FAST Ethernet Media Dependent Interface.
	TMDS	DVI signaling used for HDMI display interfaces.
	USB	DC coupled differential signaling used for traditional (non-Super-Speed) USB signals
	GND	Digital ground.
	RSV	Reserved.
	NC	No connected. This pin should be floating.
TYPE	Indicates pin type.	
	Power	Power signal.
	I CMOS	CMOS input pin.
	O CMOS	CMOS output pin.
	I/O CMOS	CMOS input and output pin.
	O OD CMOS	Open drain output pin.
	I/O OD CMOS	Open drain input and output pin.
	NC	No connected. This pin should be floating.
MAIN FUNCTION	Main or suggested function.	
COMMENTS	Clarification for the related SMARC-314 interface pin. See device chapter for more information.	

Table 4 SMARC expansion interface information

COLORS	INFORMATION
	Power Sources (Supply Voltages)
	Signal Level Voltage (Digital and Analog Ground)
	Control Signals
	Ethernet
	USB connections
	I2C
	SPI
	Wifi/Bluetooth and SD/SD card interface
	UART
	I2S
	LVDS
	HDMI
	SATA signals
	MIPI-DSI
	MIPI-CSI
	PCIe
	CAN bus
	GPIO
	PWM signals
	RTC Battery

Table 5 Colors Key

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Pin	Voltage level	Type	Main Function	Comments
Primary (Top) Side				
P1	NC	NC	PCAM_PXL_CK1	No connected
P2	GND	POWER	GND	Digital Ground
P3	LVDS D-PHY	I CMOS	CSI1_CK+ / PCAM_D0	CSI1 differential clock input +
P4	LVDS D-PHY	I CMOS	CSI1_CK- / PCAM_D1	CSI1 differential clock input -
P5	NC	NC	PCAM_DE	No connected
P6	NC	NC	PCAM_MCK	No connected
P7	LVDS D-PHY	I CMOS	CSI1_D0+ / PCAM_D2	CSI1 differential data input D0 +
P8	LVDS D-PHY	I CMOS	CSI1_D0- / PCAM_D3	CSI1 differential data input D0 -
P9	GND	POWER	GND	Digital Ground
P10	LVDS D-PHY	I CMOS	CSI1_D1+ / PCAM_D4	CSI1 differential data inputs D1 +
P11	LVDS D-PHY	I CMOS	CSI1_D1- /PCAM_D5	CSI1 differential data inputs D1 -
P12	GND	POWER	GND	Digital Ground
P13	LVDS D-PHY	I CMOS	CSI1_D2+ / PCAM_D6	CSI1 differential data input D2 +
P14	LVDS D-PHY	I CMOS	CSI1_D2- / PCAM_D7	CSI1 differential data input D2 -
P15	GND	POWER	GND	Digital Ground
P16	LVDS D-PHY	I CMOS	CSI1_D3+ / PCAM_D8	CSI1 differential data input D3 +
P17	LVDS D-PHY	I CMOS	CSI1_D3- / PCAM_D9	CSI1 differential data input D3 -
P18	GND	POWER	GND	Digital Ground
P19	GBE MDI	I/O CMOS	GBE_MDI3-	GB Ethernet pair 3 to magnetics (Media Dependent Interface).
P20	GBE MDI	I/O CMOS	GBE_MDI3+	GB Ethernet pair 3 to magnetics (Media Dependent Interface).
P21	1V8	I/O OD CMOS	GBE_LINK100#	Active Low. Link Speed Indication LED for GBE0 1000/100 Mbps speed. Inactive if 10 Mbps.
P22	NC	NC	GBE_LINK1000#	No connected
P23	GBE MDI	I/O CMOS	GBE_MDI2-	GB Ethernet pair 2 to magnetics (Media Dependent Interface).
P24	GBE MDI	I/O CMOS	GBE_MDI2+	GB Ethernet pair 2 to magnetics (Media Dependent Interface).
P25	1V8	I/O OD CMOS	GBE_LINK_ACT#	Active Low. Indicates valid link and blinks when there is activity.
P26	GBE MDI	I/O CMOS	GBE_MDI1-	GB Ethernet pair 1 to magnetics (Media Dependent Interface).
P27	GBE MDI	I/O CMOS	GBE_MDI1+	GB Ethernet pair 1 to magnetics (Media Dependent Interface).
P28	NC	NC	GBE_CTREF	No connected

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P29	GBE MDI	I/O CMOS	GBE_MDI0-	GB Ethernet pair 0 to magnetics (Media Dependent Interface).
P30	GBE MDI	I/O CMOS	GBE_MDI0+	GB Ethernet pair 0 to magnetics (Media Dependent Interface).
P31	1V8	O CMOS	SPI0_CS1#	iMX6 SPI3 chip select 2 signal
P32	GND	POWER	GND	Digital Ground
P33	3V3	I OD CMOS	SDIO_WP	MMC1 Write Protect. This signal has a 3K3 PU resistor.
P34	3V3	I/O CMOS	SDIO_CMD	MMC1 Command
P35	3V3	I OD CMOS	SDIO_CD#	MMC1 Card Detect. This signal has a 3K3 PU resistor.
P36	3V3	O CMOS	SDIO_CK	MMC1 Clock
P37	3V3	O CMOS	SDIO_PWR_EN	MMC1 Card Power Enable
P38	GND	POWER	GND	Digital Ground
P39	3V3	IO CMOS	SDIO_D0	MMC1 Data Bus 0
P40	3V3	IO CMOS	SDIO_D1	MMC1 Data Bus 1
P41	3V3	IO CMOS	SDIO_D2	MMC1 Data Bus 2
P42	3V3	IO CMOS	SDIO_D3	MMC1 Data Bus 3
P43	1V8	O CMOS	SPI0_CS0#	iMX6 SPI3 chip select 1 signal
P44	1V8	O CMOS	SPI0_CK	iMX6 SPI3 clock
P45	1V8	I CMOS	SPI0_DIN	iMX6 SPI3 Master Input-Slave Output (MISO)
P46	1V8	O CMOS	SPI0_DO	iMX6 SPI3 Master Output-Slave Input (MOSI)
P47	GND	POWER	GND	Digital Ground
P48	DS	SATA 3 Gb/s	SATA_TX+	Differential SATA transmit data +. This signal has a 10 nF coupling capacitor.
P49	DS	SATA 3 Gb/s	SATA_TX-	Differential SATA transmit data -. This signal has a 10 nF coupling capacitor.
P50	GND	POWER	GND	Digital Ground
P51	DS	SATA 3 Gb/s	SATA_RX+	Differential SATA receive data +. This signal has a 10 nF coupling capacitor.
P52	DS	SATA 3 Gb/s	SATA_RX-	Differential SATA receive data -. This signal has a 10 nF coupling capacitor.
P53	GND	POWER	GND	Digital Ground
P54	1V8	O CMOS	SPI1_CS0#	iMX6 SPI2 chip select 0 signal
P55	1V8	O CMOS	SPI1_CS1#	iMX6 SPI2 chip select 1 signal
P56	1V8	O CMOS	SPI1_CK	iMX6 SPI2 clock
P57	1V8	I CMOS	SPI1_DIN	iMX6 SPI2 Master Input-Slave Output (MISO)

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P58	1V8	O CMOS	SPI1_DO	iMX6 SPI2 Master Output-Slave Input (MOSI)
P59	GND	POWER	GND	Digital Ground
P60	USB	I/O CMOS	USB0+	USB1-OTG: USB2.0 differential data input
P61	USB	I/O CMOS	USB0-	USB1-OTG: USB2.0 differential data input
P62	3V3	IO OD CMOS	USB0_EN_OC#	USB1-OTG: Enable (active High)-Overcurrent (active low). This signal has a 3K3 PU resistor.
P63	5V	I CMOS	USB0_VBUS_DET	USB1-OTG: USB host power detection, when this port is used as a device.
P64	3V3	I CMOS	USB0_OTG_ID	USB1-OTG: Input Pin to Announce OTG ID (Device Insertion) on USB 2.0 Port, active high.
P65	USB	I/O CMOS	USB1+	USB2: USB2.0 differential data input
P66	USB	I/O CMOS	USB1-	USB2: USB2.0 differential data input
P67	3V3	IO OD CMOS	USB1_EN_OC#	USB2: Enable (active High)-Overcurrent (active low).
P68	GND	POWER	GND	Digital Ground
P69	NC	NC	USB2+	No connected
P70	NC	NC	USB2-	No connected
P71	NC	NC	USB2_EN_OC#	No connected
P72	NC	NC	PCIE_C_PRSNT#	No connected
P73	NC	NC	PCIE_B_PRSNT#	No connected
P74	3V3	I CMOS	PCIE_A_PRSNT#	PCIe Port A: Hotplug presence detect. Active low. Active low
P75	3V3	O CMOS	PCIE_A_RST#	PCIe Port A: Port reset output. Active low.
P76	NC	NC	PCIE_C_CKREQ#	No connected
P77	NC	NC	PCIE_B_CKREQ#	No connected
P78	3V3	I CMOS	PCIE_A_CKREQ#	PCIe Port A: clock request input. Active low
P79	GND	POWER	GND	Digital Ground
P80	NC	NC	PCIE_C_REFCK+	No connected
P81	NC	NC	PCIE_C_REFCK-	No connected
P82	GND	POWER	GND	Digital Ground
P83	LVDS PCIe	O CMOS	PCIE_A_REFCK+	PCIeA: Differential PCIe Link A reference clock output DC coupled.
P84	LVDS PCIe	O CMOS	PCIE_A_REFCK-	PCIeA: Differential PCIe Link A reference clock output DC coupled.
P85	GND	POWER	GND	Digital Ground
P86	LVDS PCIe	I CMOS	PCIE_A_RX+	PCIeA: Differential PCIe Link A receive data pair 0.
P87	LVDS PCIe	I CMOS	PCIE_A_RX-	PCIeA: Differential PCIe Link A receive data pair 0.

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P88	GND	POWER	GND	Digital Ground
P89	LVDS PCIe	O CMOS	PCIE_A_TX+	PCIeA: Differential PCIe Link A transmit data pair 0. This signal has a 0.1 uF coupling capacitor.
P90	LVDS PCIe	O CMOS	PCIE_A_TX-	PCIeA: Differential PCIe Link A transmit data pair 0. This signal has a 0.1 uF coupling capacitor.
P91	GND	POWER	GND	Digital Ground
P92	TMDS HDMI	O CMOS	HDMI_D2+	HDMI differential pair data input D2 +
P93	TMDS HDMI	O CMOS	HDMI_D2-	HDMI differential pair data input D2 -
P94	GND	POWER	GND	Digital Ground
P95	TMDS HDMI	O CMOS	HDMI_D1+	HDMI differential pair data input D1 +
P96	TMDS HDMI	O CMOS	HDMI_D1-	HDMI differential pair data input D1 -
P97	GND	POWER	GND	Digital Ground
P98	TMDS HDMI	O CMOS	HDMI_D0+	HDMI differential pair data input D0 +
P99	TMDS HDMI	O CMOS	HDMI_D0-	HDMI differential pair data input D0 -
P100	GND	POWER	GND	Digital Ground
P101	TMDS HDMI	O CMOS	HDMI_CK+	HDMI differential clock output pair +
P102	TMDS HDMI	O CMOS	HDMI_CK-	HDMI differential clock output pair -
P103	GND	POWER	GND	Digital Ground
P104	1V8	I CMOS	HDMI_HPD	HDMI Hot Plug Detect input. Active low
P105	1V8	I/O OD CMOS	HDMI_CTRL_CK	I2C2 clock line dedicated to HDMI.
P106	1V8	I/O OD CMOS	HDMI_CTRL_DAT	I2C2 bus data dedicated to HDMI. 0x08 is used.
P107	1V8	I/O CMOS	HDMI_CEC	HDMI Consumer Electronics Control. Active low
P108	1V8	IO CMOS	GPIO0 / CAM0_PWR#	General purpose input/output
P109	1V8	IO CMOS	GPIO1 / CAM1_PWR#	General purpose input/output
P110	1V8	IO CMOS	GPIO2 / CAM0_RST#	General purpose input/output
P111	1V8	IO CMOS	GPIO3 / CAM1_RST#	General purpose input/output
P112	1V8	IO CMOS	GPIO4 / HDA_RST#	General purpose input/output
P113	1V8	IO CMOS	GPIO5 / PWM_OUT	PMW Output 1 or General purpose input/output
P114	1V8	IO CMOS	GPIO6 / TACHIN	General purpose input/output
P115	1V8	IO CMOS	GPIO7 / PCAM_FLD	General purpose input/output
P116	1V8	IO CMOS	GPIO8 / CAN0_ERR#	General purpose input/output
P117	1V8	IO CMOS	GPIO9 / CAN1_ERR#	General purpose input/output

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P118	1V8	IO CMOS	GPIO10	General purpose input/output
P119	1V8	IO CMOS	GPIO11	General purpose input/output
P120	GND	POWER	GND	Digital Ground
P121	1V8	IO	I2C_PM_CK	Power management I2C2 bus clock.
P122	1V8	IO	I2C_PM_DAT	Power management I2C2 bus data. 0x08 is used.
P123	1V8	I OD CMOS	BOOT_SEL0#	Input straps determine the Module boot device. Active low. See table Table 9.
P124	1V8	I OD CMOS	BOOT_SEL1#	Input straps determine the Module boot device. Active low. See table Table 9.
P125	1V8	I OD CMOS	BOOT_SEL2#	Input straps determine the Module boot device. Active low. See table Table 9.
P126	1V8	OUT	RESET_OUT#	General purpose reset output to Carrier board. Active low
P127	1V8	IN	RESET_IN#	Reset input from Carrier board. Active low
P128	1V8	IN	POWER_BTN#	Power-button input from Carrier board. Active low
P129	NC	NC	SER0_TX	No connected
P130	NC	NC	SER0_RX	No connected
P131	NC	NC	SER0_RTS#	No connected
P132	NC	NC	SER0_CTS#	No connected
P133	GND	POWER	GND	Digital Ground
P134	1V8	O CMOS	SER1_TX	UART2: Asynchronous serial port 2 data out.
P135	1V8	I CMOS	SER1_RX	UART2: Asynchronous serial port 2 data in.
P136	1V8	O CMOS	SER2_TX	UART2: Asynchronous serial port 3 data out.
P137	1V8	I CMOS	SER2_RX	UART2: Asynchronous serial port 3 data in.
P138	1V8	O CMOS	SER2_RTS#	UART3: Request to Send handshake line. Active low. CTSn Output
P139	1V8	I CMOS	SER2_CTS#	UART3: Clear to Send handshake line. Active low. RTSn Input
P140	1V8	O CMOS	SER3_TX	UART4: Asynchronous serial port 4 data out.
P141	1V8	I CMOS	SER3_RX	UART4: Asynchronous serial port 4 data in.
P142	GND	POWER	GND	Digital Ground
P143	1V8	O CMOS	CAN0_TX	CAN1 Transmission line
P144	1V8	I CMOS	CAN0_RX	CAN1 Reception line
P145	1V8	O CMOS	CAN1_TX	CAN2 Transmission line
P146	1V8	I CMOS	CAN1_RX	CAN2 Reception line
P147	5V	POWER	VDD_IN0	

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P148	5V	POWER	VDD_IN1	Pins used to power up the module. Source voltage should be between 3V-5.25V
P149	5V	POWER	VDD_IN2	
P150	5V	POWER	VDD_IN3	
P151	5V	POWER	VDD_IN4	
P152	5V	POWER	VDD_IN5	
P153	5V	POWER	VDD_IN6	
P154	5V	POWER	VDD_IN7	
P155	5V	POWER	VDD_IN8	
P156	5V	POWER	VDD_IN9	
Secondary (Bottom) Side				
S1	NC	NC	PCAM_VSYNC	No connected
S2	NC	NC	PCAM_HSYNC	No connected
S3	GND	POWER	GND	Digital Ground
S4	NC	NC	PCAM_PXL_CK0	No connected
S5	1V8	IO OD CMOS	I2C_CAM_CK	I2C4 bus clock. Serial camera support link for serial cameras. Alternate function: CSI_TX+
S6	1V8	O CMOS	CAM_MCK	Master clock output for CSI camera support
S7	1V8	IO OD CMOS	I2C_CAM_DAT	I2C4 bus data. Serial camera support link for serial cameras. Alternate function: CSI_TX-
S8	NC	NC	CSI0_CK+ / PCAM_D10	No connected
S9	NC	NC	CSI0_CK- / PCAM_D11	No connected
S10	GND	POWER	GND	Digital Ground
S11	NC	NC	CSI0_D0+ / PCAM_D12	No connected
S12	NC	NC	CSI0_D0- / PCAM_D13	No connected
S13	GND	POWER	GND	Digital Ground
S14	NC	NC	CSI0_D1+ / PCAM_D14	No connected
S15	NC	NC	CSI0_D1- / PCAM_D15	No connected
S16	GND	POWER	GND	Digital Ground
S17	NC	NC	AFB0_OUT	No connected
S18	1V8	O CMOS	AFB1_OUT	PWM output 3
S19	NC	NC	AFB2_OUT	No connected
S20	NC	NC	AFB3_IN	No connected

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S21	NC	NC	AFB4_IN	No connected
S22	NC	NC	AFB5_IN	No connected
S23	NC	NC	AFB6_PTIO	No connected
S24	NC	NC	AFB7_PTIO	No connected
S25	GND	POWER	GND	Digital Ground
S26	NC	NC	SDMMC_D0	No connected
S27	NC	NC	SDMMC_D1	No connected
S28	NC	NC	SDMMC_D2	No connected
S29	NC	NC	SDMMC_D3	No connected
S30	NC	NC	SDMMC_D4	No connected
S31	NC	NC	SDMMC_D5	No connected
S32	NC	NC	SDMMC_D6	No connected
S33	NC	NC	SDMMC_D7	No connected
S34	GND	POWER	GND	Digital Ground
S35	NC	NC	SDMMC_CK	No connected
S36	NC	NC	SDMMC_CMD	No connected
S37	NC	NC	SDMMC_RST#	No connected
S38	1V8	O CMOS	AUDIO_MCK	Master clock output to Audio codecs
S39	1V8	I/O CMOS	I2S0_LRCK	SAI1: iMX6 AUD4 Transmit Frame Sync signal
S40	1V8	O CMOS	I2S0_SDOUT	SAI1: iMX6 AUD4 Data Transmit signal
S41	1V8	I CMOS	I2S0_SDIN	SAI1: iMX6 AUD4 Data Receive signal
S42	1V8	I/O CMOS	I2S0_CK	SAI1: iMX6 AUD4 Transmit Clock signal
S43	NC	NC	I2S1_LRCK	No connected
S44	NC	NC	I2S1_SDOUT	No connected
S45	NC	NC	I2S1_SDIN	No connected
S46	NC	NC	I2S1_CK	No connected
S47	GND	POWER	GND	Digital Ground
S48	1V8	I/O CMOS	I2C_GP_CK	I2C3 bus clock. Active low..
S49	1V8	I/O CMOS	I2C_GP_DAT	I2C3 bus data. 0x50 is used. Active low.
S50	NC	NC	I2S2_LRCK	No connected
S51	NC	NC	I2S2_SDOUT	No connected

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S52	NC	NC	I2S2_SDIN	No connected
S53	NC	NC	I2S2_CK	No connected
S54	3V3	O CMOS	SATA_ACT#	Active low SATA activity indicator
S55	NC	NC	AFB8_PTIO	No connected
S56	NC	NC	AFB9_PTIO	No connected
S57	NC	NC	PCAM_ON_CSI0#	No connected
S58	NC	NC	PCAM_ON_CSI1#	No connected
S59	NC	NC	SPDIF_OUT	No connected
S60	NC	NC	SPDIF_IN	No connected
S61	GND	POWER	GND	Digital Ground
S62	NC	NC	AFB_DIFF0+	No connected
S63	NC	NC	AFB_DIFF0-	No connected
S64	GND	POWER	GND	Digital Ground
S65	NC	NC	AFB_DIFF1+	No connected
S66	NC	NC	AFB_DIFF1-	No connected
S67	GND	POWER	GND	Digital Ground
S68	DS	I/O CMOS	AFB_DIFF2+	DSI0: clock differential pair +
S69	DS	I/O CMOS	AFB_DIFF2-	DSI0: clock differential pair -
S70	GND	POWER	GND	Digital Ground
S71	DS	O CMOS	AFB_DIFF3+	DSI0: data differential pair D0 +
S72	DS	O CMOS	AFB_DIFF3-	DSI0: data differential pair D0 -
S73	GND	POWER	GND	Digital Ground
S74	DS	O CMOS	AFB_DIFF4+	DSI0: data differential pair D1 +
S75	DS	O CMOS	AFB_DIFF4-	DSI0: data differential pair D1 -
S76	NC	NC	PCIE_B_RST#	No connected
S77	NC	NC	PCIE_C_RST#	No connected
S78	NC	NC	PCIE_C_RX+	No connected
S79	NC	NC	PCIE_C_RX-	No connected
S80	GND	POWER	GND	Digital Ground
S81	NC	NC	PCIE_C_TX+	No connected
S82	NC	NC	PCIE_C_TX-	No connected

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S83	GND	POWER	GND	Digital Ground
S84	NC	NC	PCIE_B_REFCK+	No connected
S85	NC	NC	PCIE_B_REFCK-	No connected
S86	GND	POWER	GND	Digital Ground
S87	NC	NC	PCIE_B_RX+	No connected
S88	NC	NC	PCIE_B_RX-	No connected
S89	GND	POWER	GND	Digital Ground
S90	NC	NC	PCIE_B_TX+	No connected
S91	NC	NC	PCIE_B_TX-	No connected
S92	GND	POWER	GND	Digital Ground
S93	NC	NC	LCD_D0	No connected
S94	NC	NC	LCD_D1	No connected
S95	NC	NC	LCD_D2	No connected
S96	NC	NC	LCD_D3	No connected
S97	NC	NC	LCD_D4	No connected
S98	NC	NC	LCD_D5	No connected
S99	NC	NC	LCD_D6	No connected
S100	NC	NC	LCD_D7	No connected
S101	GND	POWER	GND	Digital Ground
S102	NC	NC	LCD_D8	No connected
S103	NC	NC	LCD_D9	No connected
S104	NC	NC	LCD_D10	No connected
S105	NC	NC	LCD_D11	No connected
S106	NC	NC	LCD_D12	No connected
S107	NC	NC	LCD_D13	No connected
S108	NC	NC	LCD_D14	No connected
S109	NC	NC	LCD_D15	No connected
S110	GND	POWER	GND	Digital Ground
S111	NC	NC	LCD_D16	No connected
S112	NC	NC	LCD_D17	No connected
S113	NC	NC	LCD_D18	No connected

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S114	NC	NC	LCD_D19	No connected
S115	NC	NC	LCD_D20	No connected
S116	NC	NC	LCD_D21	No connected
S117	NC	NC	LCD_D22	No connected
S118	NC	NC	LCD_D23	No connected
S119	GND	POWER	GND	Digital Ground
S120	NC	NC	LCD_DE	No connected
S121	NC	NC	LCD_VS	No connected
S122	NC	NC	LCD_HS	No connected
S123	NC	NC	LCD_PCK	No connected
S124	GND	POWER	GND	Digital Ground
S125	DS	O CMOS	LVDS0+	LVDS data channel differential pair D0 +
S126	DS	O CMOS	LVDS0-	LVDS data channel differential pair D0 -
S127	1V8	I/O CMOS	LCD_BKLT_EN	High enables panel backlight
S128	DS	O CMOS	LVDS1+	LVDS data channel differential pair D1+
S129	DS	O CMOS	LVDS1-	LVDS data channel differential pair D1 -
S130	GND	POWER	GND	Digital Ground
S131	DS	O CMOS	LVDS2+	LVDS data channel differential pair D2 +
S132	DS	O CMOS	LVDS2-	LVDS data channel differential pair D2 -
S133	1V8	I/O CMOS	LCD_VDD_EN	High enables panel VDD
S134	DS	O CMOS	LVDS_CK+	LVDS clock channel differential pair +
S135	DS	O CMOS	LVDS_CK-	LVDS clock channel differential pair -
S136	GND	POWER	GND	Digital Ground
S137	DS	O CMOS	LVDS3+	LVDS data channel differential pair D3 +
S138	DS	O CMOS	LVDS3-	LVDS data channel differential pair D3 -
S139	1V8	IO CMOS	I2C_LCD_CK	I2C4 bus clock. This signal has a 1K5 PU resistor. Solo/DualLite version. I2C1 bus clock. This signal has a 1K5 PU resistor. Dual/Quad version.
S140	1V8	IO CMOS	I2C_LCD_DAT	I2C4 bus data. This signal has a 1K5 PU resistor. Solo/DualLite version. I2C1 bus data. This signal has a 1K5 PU resistor. Dual/Quad version.

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S141	1V8	O CMOS	LCD_BKLT_PWM	Display Backlight. PMW output 4.
S142	NC	NC	RSVD	No connected
S143	GND	POWER	GND	Digital Ground
S144	NC	NC	RSVD / EDP_HPD	No connected
S145	1V8	O CMOS	WDT_TIME_OUT#	Watch-Dog-Timer Output
S146	3V3	I CMOS	PCIE_WAKE#	PCIe wake up interrupt to host. This signal has a 4K7 PU resistor.
S147	VBAT	I/O CMOS	VDD_RTC	Low current RTC circuit backup power. Voltages from 2.5V to 3.3V.
S148	1V8	I CMOS	LID#	Lid open/close indication to Module. Active low.
S149	1V8	I CMOS	SLEEP#	Sleep indicator from Carrier board. Active low.
S150	5V	I CMOS	VIN_PWR_BAD#	Power bad indication from Carrier board. Active low.
S151	1V8	I CMOS	CHARGING#	Held low by Carrier during battery charging. Active low.
S152	1V8	I CMOS	CHARGER_PRSNT#	Held low by Carrier if DC input for battery charger is present. Active low.
S153	1V8	O CMOS	CARRIER_STBY#	The Module shall drive this signal low when the system is in a standby power state. Active high.
S154	1V8	O CMOS	CARRIER_PWR_ON	Carrier board circuits (apart from power management and power path circuits) should not be Powered up until the Module asserts the CARRIER_PWR_ON signal.
S155	1V8	I CMOS	FORCE_RECOV#	Low on this pin disable boot select circuit. Active low.
S156	1V8	I CMOS	BATLOW#	Battery low indication to Module. Active low.
S157	1V8	I CMOS	TEST#	Held low by Carrier to invoke Module vendor specific test function(s). Active low.
S158	GND	POWER	GND	Digital Ground

Table 6 SMARC pinout description

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5 PRODUCT SPECIFICATIONSUMMARY

5.1 POWER SOURCES

5.1.1 Supply Voltage

The power supply of the module is made with a single standard voltage of 5V, using the defined inputs (pins P147 to P156, all the connections in this chapter are referred to the SMARC-314 connector, see Table 7 Power Supply pins). This voltage can be from a minimum value of 3V to a maximum of 5.25V (see resume of electrical characteristics in Chapter 7: ELECTRICAL CHARACTERISTICS). Next figure shows a schematic example of this power signal (page 88 of SMARC Design Guide).

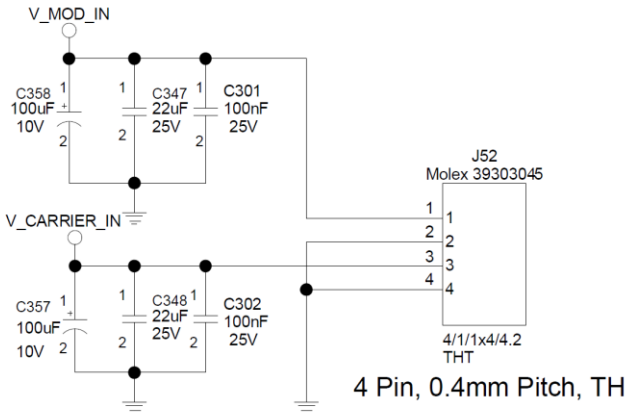

Figure 15 Power Supply Input circuit

Pin	Volt Level	Type	Main Function	Comments
5V Input Power				
P147	5V	Power	VDD_IN0	Pins used to power up the module. Source voltage should be between 3V to 5V25
P148	5V	Power	VDD_IN1	Pins used to power up the module. Source voltage should be between 3V to 5V25
P149	5V	Power	VDD_IN2	Pins used to power up the module. Source voltage should be between 3V to 5V25
P150	5V	Power	VDD_IN3	Pins used to power up the module. Source voltage should be between 3V to 5V25
P151	5V	Power	VDD_IN4	Pins used to power up the module. Source voltage should be between 3V to 5V25
P152	5V	Power	VDD_IN5	Pins used to power up the module. Source voltage should be between 3V to 5V25
P153	5V	Power	VDD_IN6	Pins used to power up the module. Source voltage should be between 3V to 5V25
P154	5V	Power	VDD_IN7	Pins used to power up the module. Source voltage should be between 3V to 5V25
P155	5V	Power	VDD_IN8	Pins used to power up the module. Source voltage should be between 3V to 5V25
P156	5V	Power	VDD_IN9	Pins used to power up the module. Source voltage should be between 3V to 5V25

Table 7 Power Supply pins

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5.1.2 Digital Ground

All the GND pins are internally connected together, so it's not needed to connect all of them. However, the user has to considerer how many of them connect according to the total consumption of the complete circuit (the IGEP™ SMARC iMX6 and the base board developed). At the same time, to make the routing of buses easier, the ground connection chosen will be the nearest to the function used.

Pin	Volt Level	Type	Main Function	Comments
Digital Ground				
P2	GND	Power	GND	Digital ground
P9	GND	Power	GND	Digital ground
P12	GND	Power	GND	Digital ground
P15	GND	Power	GND	Digital ground
P18	GND	Power	GND	Digital ground
P32	GND	Power	GND	Digital ground
P38	GND	Power	GND	Digital ground
P47	GND	Power	GND	Digital ground
P50	GND	Power	GND	Digital ground
P53	GND	Power	GND	Digital ground
P59	GND	Power	GND	Digital ground
P68	GND	Power	GND	Digital ground
P79	GND	Power	GND	Digital ground
P82	GND	Power	GND	Digital ground
P85	GND	Power	GND	Digital ground
P88	GND	Power	GND	Digital ground
P91	GND	Power	GND	Digital ground
P94	GND	Power	GND	Digital ground
P97	GND	Power	GND	Digital ground
P100	GND	Power	GND	Digital ground
P103	GND	Power	GND	Digital ground
P120	GND	Power	GND	Digital ground
P133	GND	Power	GND	Digital ground
P142	GND	Power	GND	Digital ground

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S3	GND	Power	GND	Digital ground
S10	GND	Power	GND	Digital ground
S13	GND	Power	GND	Digital ground
S16	GND	Power	GND	Digital ground
S25	GND	Power	GND	Digital ground
S34	GND	Power	GND	Digital ground
S47	GND	Power	GND	Digital ground
S61	GND	Power	GND	Digital ground
S64	GND	Power	GND	Digital ground
S67	GND	Power	GND	Digital ground
S70	GND	Power	GND	Digital ground
S73	GND	Power	GND	Digital ground
S80	GND	Power	GND	Digital ground
S83	GND	Power	GND	Digital ground
S86	GND	Power	GND	Digital ground
S89	GND	Power	GND	Digital ground
S92	GND	Power	GND	Digital ground
S101	GND	Power	GND	Digital ground
S110	GND	Power	GND	Digital ground
S119	GND	Power	GND	Digital ground
S124	GND	Power	GND	Digital ground
S130	GND	Power	GND	Digital ground
S136	GND	Power	GND	Digital ground
S143	GND	Power	GND	Digital ground
S158	GND	Power	GND	Digital ground

Table 8 Digital Ground pins

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5.2 CONTROL SIGNALS

There are different pins used as general control signals. They affect the *Boot Mode*, the management of the power supply and resets.

5.2.1 Boot Modes

The Boot Mode can be fixed by user acting over the pins P125, P124 and P123. When the module is powered on, it reads these pins, and it boots as it is specified in next table.

BOOT_SEL2# (P125)	BOOT_SEL2# (P124)	BOOT_SEL2# (P123)	Boot source
GND	GND	GND	Reserved
GND	GND	Float	Carrier SD Card
GND	Float	GND	Carrier eMMC Flash
GND	Float	Float	Carrier SPI
Float	GND	GND	Module device
Float	GND	Float	Remote boot
Float	Float	GND	Reserved
Float	Float	Float	Reserved

Table 9 Boot Mode

Reserved positions are combinations which are not implemented in current SMARC module. Users must avoid using them since it would not be possible to complete a module boot up.

Please, be careful that **default position is '111'.** This is a reserved position, and it is not possible to perform a complete module boot up since there is not an implemented Flash-SPI at Boot instructions. The User must use any of available combinations. In example, it is possible to boot from a SD-Card using combination '001'.

It is recommended to use a jumper header or a switch in series with a low resistor value (as a short circuit protector element) tied to GND in Carrier Board to control the values of these boot pins as it is showed in next figure (page 29 of SMARC Design Guide).

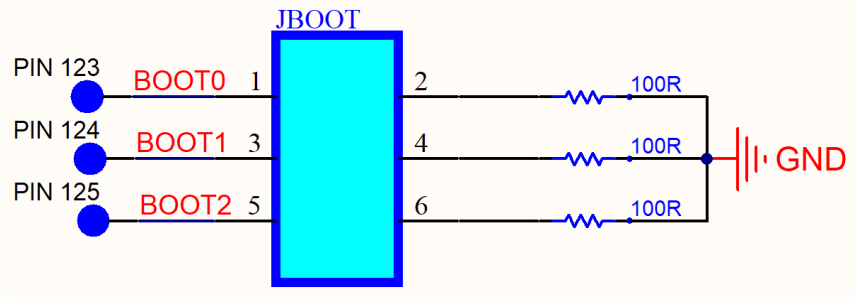

Figure 16 Boot Mode: jumpers selectors

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5.2.2 Reset pins

There are two available Reset pins in the module for general purposes.

- **RESET_OUT# (P126)** - General purpose reset output to Carrier Board, active Low. Connected to GPIO6_IO05 (iMX6 ball L6).
- **RESET_IN# (P127)** - Reset input from Carrier Board, connected to PMIC control. Active Low. In this case, when it is low state, Carrier forces a Module Reset.

5.2.3 External Pushbutton

- **Power-button input**

POWER_BTN# (P128) - Power-button input from Carrier board, active Low. Connected to GPIO6_IO00 (iMX6 ball M4).

5.2.4 Module State Pins

- **Watchdog Timer output**

Pin WDT_TIME_OUT# (S145) Watchdog interrupt output. This is active low. Connected to WDOG2_B (iMX6 ball T25).

- **Lid**

Lid#(S148) – Lid open/close indication to Module. Active low. Related to GPIO6_IO03 (iMX6 ball L3).

- **Sleep**

Pin SLEEP# (S149) - Carrier drives to float the line in in-activate state. Active low, level sensitive. Pulled up on Module. Driven by OD part on Carrier. Related to GPIO6_02(iMX6 processor ball L4).

- **VIN_PWR_BAD**

VIN_PWR_BAD# (S151) – Allows to disable the 1V8 LDOs in order to deactivate several peripherals. This signal is normally floating, in order to disable the 1V8 LDOs and active the signal you should hold VIN_PWR_BAD# to GND. In the figure below you could see an example of how control the signal VIN_PWR_BAD through a transistor.

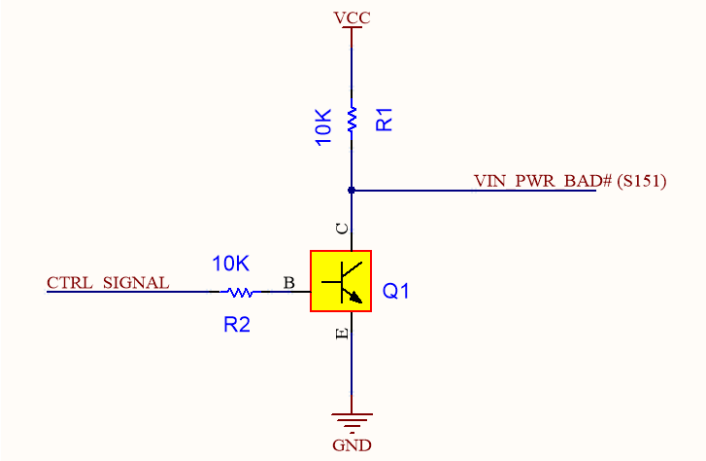

Figure 17 VIN_PWR_BAD circuit Example (Vcc =Vin).

- **Charging**

Pin CHARGING#(S151) - Held low by Carrier during battery charging. Active low. Related to GPIO6_IO01 (iMX6 ball M5).

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- **Charger prsnt**

Pin CHARGER_PRSNT#(S152) - Held low by Carrier if DC input for battery charger is present. Active low. Related to GPIO4_IO16 (iMX6 ball N19).

- **Carrier Standby**

Pin CARRIER_STBY# (S153) - Signal is Low when system is in a standby power state. Related to GPIO5_07 (iMX6 processor ball R20).

- **Carrier Power On**

Pin CARRIER_PWR_ON# (S154) - Carrier board circuits (apart from power management and power path circuits) should not be powered until the Module asserts this signal. Related to GPIO3_25 (iMX6 processor ball G22).

- **Force Recovery**

Pin FORCE_RECOV# (S155) - Low on this pin disable boot select circuit.

- **Batlow**

BATLOW# (S156) - Battery low indication to Module. Related to GPIO5_13 (iMX6 processor ball U23).

- **Test**

Pin TEST# (S157) - Held low by Carrier to invoke Module test functions. Pulled up on Module. Active low. Related to GPIO3_IO16 (iMX6 processor ball C25).

The table below shows a summary of all control signals:

Pin	Volt Level	Type	Main Function	Comments
BOOT MODES				
P123	1V8	I CMOS	BOOT_SEL0#	Boot device. Active Low.
P124	1V8	I CMOS	BOOT_SEL1#	Boot device. Active Low.
P125	1V8	I CMOS	BOOT_SEL2#	Boot device. Active Low.
RESET PINS				
P126	1V8	O CMOS	RESET_OUT#	Reset out to Carrier. Active Low. nRESPWRON PIN of PMIC.
P127	1V8	I CMOS	RESET_IN#	Reset input from Carrier. Active Low. Connected to PORZ.
EXTERNAL PUSHBUTTON				
P128	1V8	I CMOS	POWER_BTN#	Power button input from Carrier Board. Active Low..
OTHER PINS				
S145	1V8	O CMOS	WDT_TIME_OUT#	Watch-Dog-Timer Output
S148	1V8	I CMOS	LID#	Lid open/close indication to Module. Active low.
S149	1V8	I CMOS	SLEEP#	Sleep signal from Carrier to PMIC.

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S150	5V	I CMOS	VIN_PWR_BAD#	Disable 1V8 module supply voltage. Active low.
S151	1V8	I CMOS	CHARGING#	Held low by Carrier during battery charging. Active low.
S152	1V8	I CMOS	CHARGER_PRSNT#	Held low by Carrier if DC input for battery charger is present. Active low.
S153	1V8	O CMOS	CARRIER_STBY#	Carrier Standby signal [GPIO FROM IOMUX P02 (I2C2)] from module to Carrier.
S154	1V8	O CMOS	CARRIER_PWR_ON#	Carrier Power ON signal to Carrier goes to GPIO IOMUX P03 (I2C2).
S155	1V8	I CMOS	FORCE_RECOVERY#	Recovery signal from Carrier to boot from serial Downloader.
S156	1V8	I CMOS	BATLOW#	Battery low indication to Module. Active low.
S157	1V8	I CMOS	TEST#	Held low by Carrier to invoke Module vendor specific test function(s). Active low.

Table 10 Control Signals pins

5.3 ETHERNET

There are two Ethernet ports in the SMARC iMX6 module: one Gigabit Ethernet (10/100/1000 Mbps). It has implemented a physical layer and a block of pins of SMARC-314 interface that can be connected directly to the Ethernet LAN. Transmission and reception lines (TX and RX) are differential (with pin function indicated as Negative and Positive) and **they should be connected to isolation magnetics**. The data lines have to be equal length and symmetric, and respect a 100 Ω differential impedance in the layout traces. The differential pairs must be isolated from nearby signals and circuitry to maintain the signal integrity.

Moreover, the magnetics module has a critical effect, so it has to be designed carefully. In order to obtain a smaller size, it is usual to use RJ45 connectors with the magnetics incorporated. If the magnetics are discrete components, they have to respect a separation under of 25 mm between them and the RJ45 connector, and 20 mm or greater between them and the SMARC-314 connector.

Gigabit Ethernet

- There is an additional port supporting Gigabit Ethernet (10/100/1000 Mbps). It also has implemented a physical layer (PHY) to be connected directly to the Ethernet LAN. Key benefits of PHY used are next:
- Compliant with IEEE802.3 (10BASE-T, 100BASE-T and 1000BASE-T) specifications.
- Supports RGMII, RMII
- Supports 1,5 V, 1,8 V, 2,5 V and 3,3 V CMOS for RGMII versions 1.3 and 2.0 (without HSTL support), as well as RMII version 1.2
- Supports a variety of clock sources: 25 MHz Xtal, 25 MHz OSC, 125 MHz OSC
- Supports programmable output frequencies of 25 MHz, 50 MHz or 125 MHz, regardless of chosen Xtal or OSC frequencies.
- Supports a wide array of stand-alone hardware configuration options.
- Supports all 5 bits of MDIO/MDC addressing possible for managed mode designs using pull-up/pull-down resistors.

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- Devices support operating temperatures of -40ºC ambient to 125ºC junction or 0ºC ambient to 125ºC junction.
- Optionally reports if a link partner is requesting inline Power-over-Ethernet (PoE and PoE+)
- Available in 6 mm x 6 mm, 48-pin QFN package.

In the next figure (page 69 of SMARC Design Guide) is shown an example of connection diagram, using a RJ45 connector with integrated magnetics.

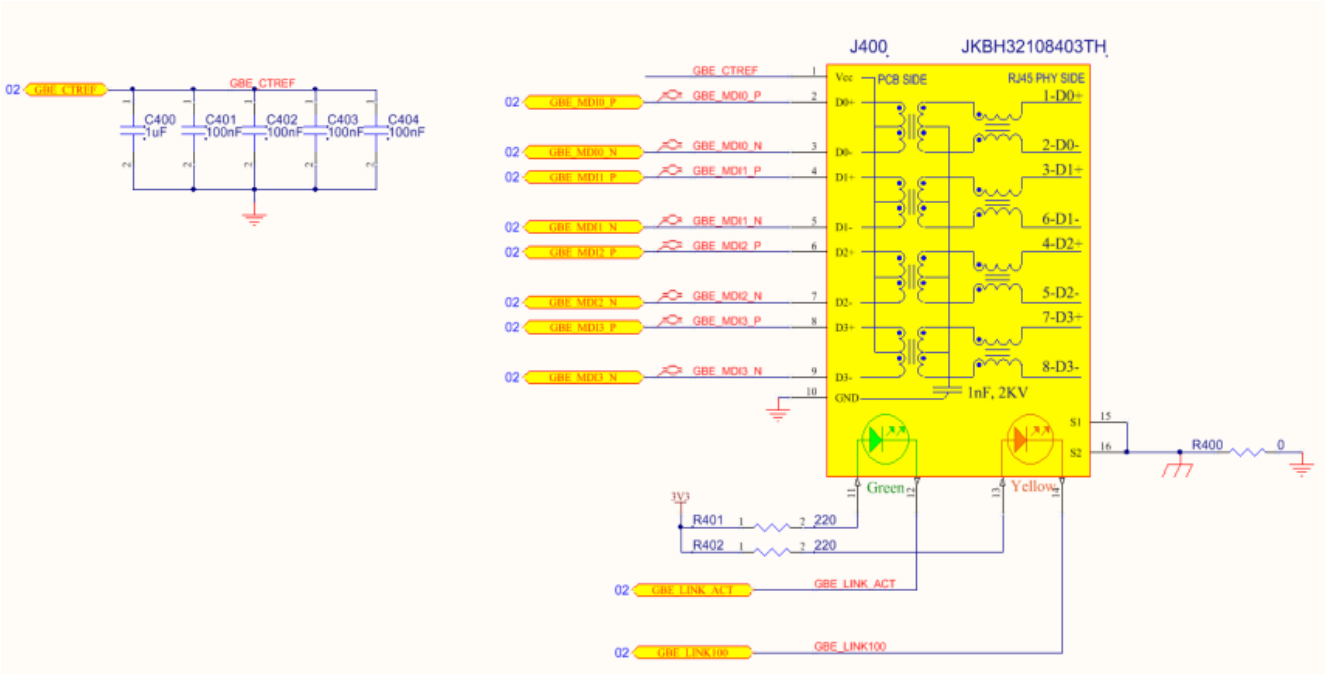

Figure 18 Ethernet 10/100/1000 Mbps standard circuit

Pin	Volt Level	Type	Main Function	Comments
P19	GBE MDI	I/O CMOS	GBE_MDI3-	GB Ethernet pair 3 to magnetics (Media Dependent Interface).
P20	GBE MDI	I/O CMOS	GBE_MDI3+	GB Ethernet pair 3 to magnetics (Media Dependent Interface).
P21	1V8	I/O OD CMOS	GBE_LINK100#	Active Low. Link Speed Indication LED for GBE0 1000/100 Mbps speed. Inactive if 10 Mbps.
P23	GBE MDI	I/O CMOS	GBE_MDI2-	GB Ethernet pair 2 to magnetics (Media Dependent Interface).
P24	GBE MDI	I/O CMOS	GBE_MDI2+	GB Ethernet pair 2 to magnetics (Media Dependent Interface).
P25	1V8	I/O OD CMOS	GBE_LINK_ACT#	Active Low. Indicates valid link and blinks when there is activity.
P26	GBE MDI	I/O CMOS	GBE_MDI1-	GB Ethernet pair 1 to magnetics (Media Dependent Interface).
P27	GBE MDI	I/O CMOS	GBE_MDI1+	GB Ethernet pair 1 to magnetics (Media Dependent Interface).
P29	GBE MDI	I/O CMOS	GBE_MDI0-	GB Ethernet pair 0 to magnetics (Media Dependent Interface).
P30	GBE MDI	I/O CMOS	GBE_MDI0+	GB Ethernet pair 0 to magnetics (Media Dependent Interface).

Table 11 Ethernet pins

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5.4 USB CONNECTIONS

There are two possibilities to connect the module to other USB devices: with a standard Host base and with an OTG (On-The-Go) interface.

The USB 2.0 Host connection is provided for connecting other devices acting as Clients of the module (for example, an external HDD). The SMARC-314 connector lines referred to this function are adapted for a USB type A receptacle, see wiring example in the next figure (page 65 of SMARC Design Guide).

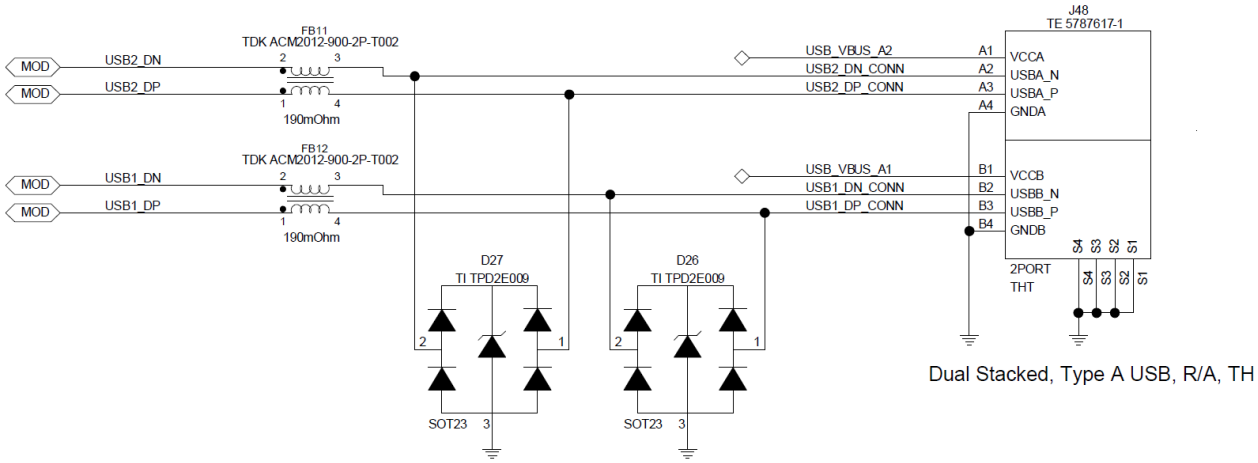

Figure 19 USB 2.0 Host connections

The USB 2.0 OTG connection allows the configuration of the board as Host or Client in function of the wire of connection used for linking both devices (the IGEP™ module and the external device; adapting the SMARC-314 connector lines for an USB type AB). It's defined by the pin P64 (USB0_OTG_ID): when the board detects this pin connected at ground, it will be an A-device; by the other side, if the pin is floating (NC) it will be a B-device. The next figure shows the connections (page 64 of SMARC Design Guide).

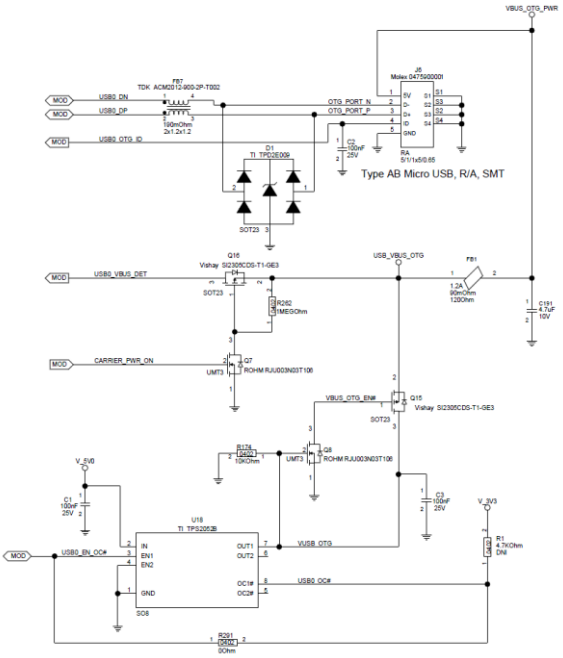

Figure 20 MicroUSB AB 2.0 OTG connections

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The USB0_EN_OC# (P62) and USB1_EN_OC# (P67) are, in both cases, optional pins used to detect if there has been an over-consumption (for example a short-circuit). Although in the second example these references are used, it's possible to apply any other of the free GPIO pins if the user wants to implement this feature.

It must be respected a 90Ω (+/-15%) differential impedance in the layout traces when the base board will be designed. At the same time, the traces have to be equal length and symmetric, with regards of shape, length and via count. The differential pairs must be isolated from nearby signals and circuitry to maintain the signal integrity.

To protect the VBUS against overcurrent, the USB power source current have to be less or equal than 500mA, and the user must provide a protection in the base board as it is showed into Figure 19 USB 2.0 Host connections and *Figure 20 MicroUSB AB 2.0 OTG connections* examples.

The following table offers the list in the SMARC-314 related pins with both of USB connections.

Pin	Volt Level	Type	Main Function	Comments
USB 2.0 OTG				
P60	USB	I/O CMOS	USB0+	USB1-OTG: USB2.0 differential data input
P61	USB	I/O CMOS	USB0-	USB1-OTG: USB2.0 differential data input
P62	3V3	IO OD CMOS	USB0_EN_OC#	USB1-OTG: Enable (active High)-Overcurrent (active low). This signal has a 3K3 PU resistor.
P63	5V	I CMOS	USB0_VBUS_DET	USB1-OTG: USB host power detection, when this port is used as a device.
P64	3V3	I CMOS	USB0_OTG_ID	USB1-OTG: Input Pin to Announce OTG ID (Device Insertion) on USB 2.0 Port, active high.
USB 2.0 Host				
P65	USB	I/O CMOS	USB1+	USB2: USB2.0 differential data input
P66	USB	I/O CMOS	USB1-	USB2: USB2.0 differential data input
P67	3V3	IO OD CMOS	USB1_EN_OC#	USB2: Enable (active High)-Overcurrent (active low).

Table 12 USB pins

5.5 I2C: INTER-INTEGRATED CIRCUIT INTERFACE

The IGEP™ SMARC iMX6 module can be connected to other peripheral devices by four I2C serial buses. There are ten pins in the SMARC-314 that may be used for this application: HDMI_CTRL_CK, HDMI_CTRL_DAT, I2C_CAM_DAT, I2C_CAM_CK, I2C_GP_DAT, I2C_GP_CK, I2C_LCD_DAT, I2C_LCD_CK, I2C_PM_DAT and I2C_PM_CK.

The IGEP SMARC iMX6 uses a 1V8 voltage levels for I2C buses. In some cases, bidirectional voltage translators should be necessary to adapt voltage levels between ICs. It is important to say that HDMI is connected to I2C1. (address 0x50)

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In the next example (page 46 of SMARC Design Guide V_IO=1V8) an example of I2C connection is shown.

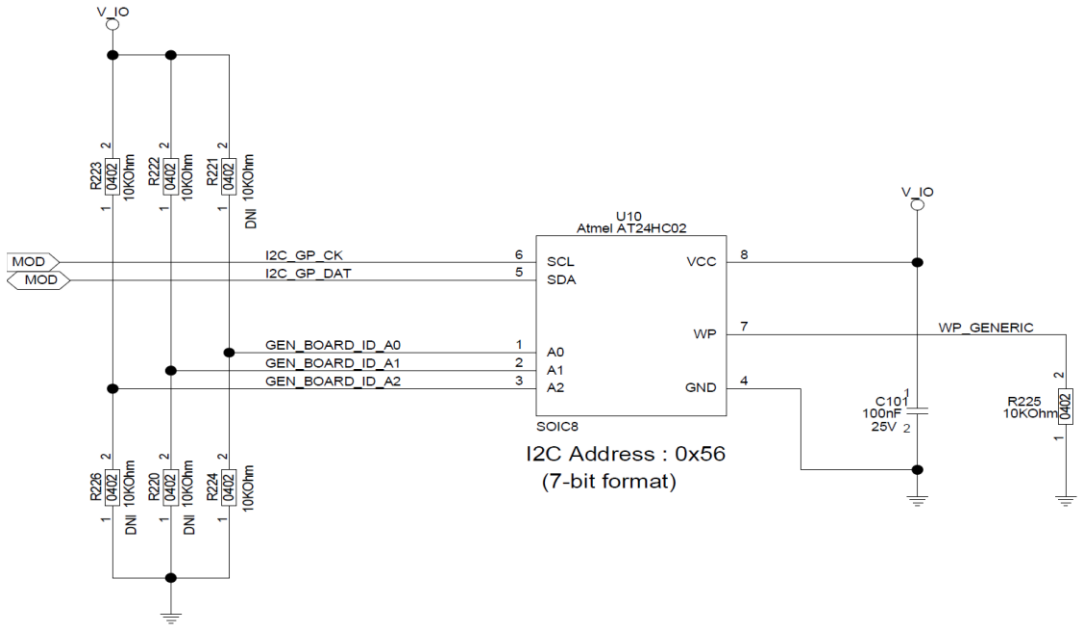

Figure 21 I2C example: EEPROM connection

Pin	Volt Level	Type	Main Function	Comments
P105	1V8	I/O OD CMOS	HDMI_CTRL_CK	I2C2 clock line dedicated to HDMI.
P106	1V8	I/O OD CMOS	HDMI_CTRL_DAT	I2C2 bus data dedicated to HDMI. 0x08 is used.
P121	1V8	IO	I2C_PM_CK	I2C2 Power management I2C2 bus clock.
P122	1V8	IO	I2C_PM_DAT	I2C2 Power management I2C2 bus data. 0x08 is used.
S5	1V8	IO OD CMOS	I2C_CAM_CK	I2C1 bus clock. Serial camera support link for serial cameras. Alternate function: CSI_TX+
S7	1V8	IO OD CMOS	I2C_CAM_DAT	I2C1 bus data. Serial camera support link for serial cameras. Alternate function: CSI_TX-
S48	1V8	I/O CMOS	I2C_GP_CK	I2C3 bus clock. Active low..
S49	1V8	I/O CMOS	I2C_GP_DAT	I2C3 bus data. 0x50 is used. Active low.
S139	1V8	IO CMOS	I2C_LCD_CK	I2C4 bus clock. This signal has a 1K5 PU resistor. Solo/DualLite version.
				I2C1 bus clock. This signal has a 1K5 PU resistor. Dual/Quad version.
S140	1V8	IO CMOS	I2C_LCD_DAT	I2C4 bus data. This signal has a 1K5 PU resistor. Solo/DualLite version.
				I2C1 bus data. This signal has a 1K5 PU resistor. Dual/Quad version.

Table 13 I2C pins

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5.6 SPI: SERIAL PERIPHERAL INTERFACE

The Serial Peripheral Interface (SPI) is one more of the different possibilities to connect the module to external peripherals. It is a full duplex synchronous bus, supporting a single master and up to two slave devices each SPI peripheral.

The IGEP™ SMARC iMX6 uses a 1V8 voltage levels for SPI buses. In some cases, voltage translators should be necessary to adapt voltage levels between ICs. It is important to say that a SPI NOR flash is connected through SPI3 and SPI3_CS0 (it is optional).

In the next figure an example is shown to connect the IGEP™ SMARC iMX6 module to an SPI Flash Socket (page 58 of SMARC Design Guide V_IO=1V8).

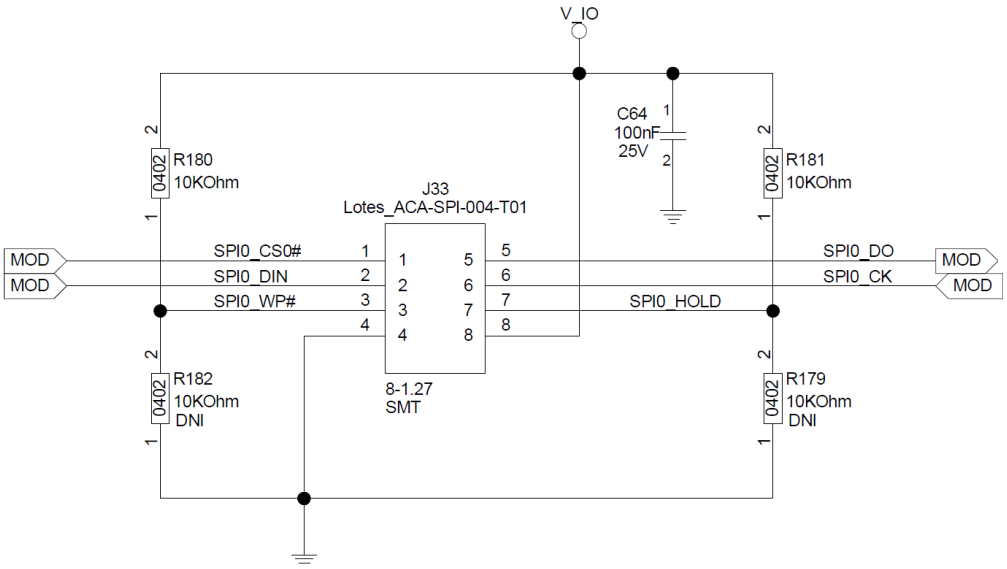

Figure 22 SPI example: SPI Flash Socket

Pin	Volt Level	Type	Main Function	Comments
SPI0				
P31	1V8	O CMOS	SPI0_CS1#	iMX6 SPI3 chip select 2 signal
P43	1V8	O CMOS	SPI0_CS0#	iMX6 SPI3 chip select 1 signal
P44	1V8	O CMOS	SPI0_CK	iMX6 SPI3 clock
P45	1V8	I CMOS	SPI0_DIN	iMX6 SPI3 Master Input-Slave Output (MISO)
P46	1V8	O CMOS	SPI0_DO	iMX6 SPI3 Master Output-Slave Input (MOSI)
SPI1				
P54	1V8	O CMOS	SPI1_CS0#	iMX6 SPI2 chip select 0 signal
P55	1V8	O CMOS	SPI1_CS1#	iMX6 SPI2 chip select 1 signal
P56	1V8	O CMOS	SPI1_CK	iMX6 SPI2 clock

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P57	1V8	I CMOS	SPI1_DIN	iMX6 SPI2 Master Input-Slave Output (MISO)
P58	1V8	O CMOS	SPI1_DO	iMX6 SPI2 Master Output-Slave Input (MOSI)

Table 14 SPI pins

5.7 WiFi/Bluetooth and SD/MMC/SDIO CARD (4 bit) INTERFACE

The SMARC iMX6 modules contains a certified high-performance WiFi/Bluetooth module with Texas Instruments chipset. Main features are next:

- IEEE 802.11 b/g/n
- Bluetooth 4.2
- Module has an internal antenna.
- Possible to use an external antenna through U.FL jack connector.
- Using external antenna, the cable connected to module must have 50 Ω impedance.

This feature uses control lines from iMX6 processor which are shared with other peripheral.

- **UART1 –** (MMC2) This is used to communicate with Bluetooth signals in the WiFi/Bluetooth module (BT_RX, BT_CTS, BT_TX and BT_RTS). If there is not implemented the WiFi/Bluetooth functionality, this can be used as SER2. When WiFi/Bluetooth is installed, these pins in the SMARC-314 interface should float.

The IGEP™ SMARC iMX6 has three MMC (Multi Media Card) interfaces. The first one (MMC1) is connected to SDIO SMARC pins (as it is shown in Table 15 MMC pins), the second one (MMC2) is used into on-board WiFi module and the third one (MMC3) is used into on-board eMMC flash.

The next example shows how to connect a uSD card reader to SDIO pins (page 78 of SMARC Design Guide).

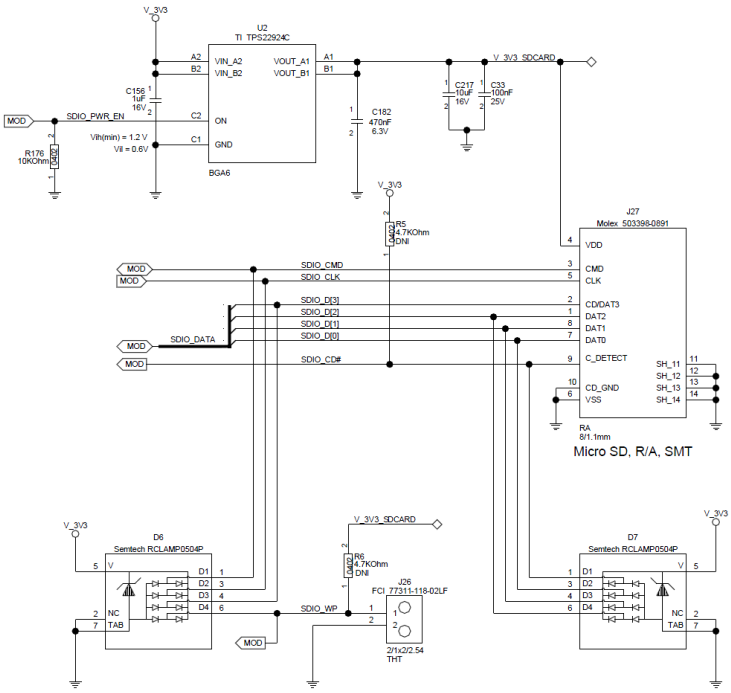

Figure 23 MMC example: uSD card reader

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Pin	Volt Level	Type	Main Function	Comments
P33	3V3	I OD CMOS	SDIO_WP	MMC1 Write Protect. This signal has a 3K3 PU resistor.
P34	3V3	I/O CMOS	SDIO_CMD	MMC1 Command
P35	3V3	I OD CMOS	SDIO_CD#	MMC1 Card Detect. This signal has a 3K3 PU resistor.
P36	3V3	O CMOS	SDIO_CK	MMC1 Clock
P37	3V3	O CMOS	SDIO_PWR_EN	MMC1 Card Power Enable
P39	3V3	IO CMOS	SDIO_D0	MMC1 Data Bus 0
P40	3V3	IO CMOS	SDIO_D1	MMC1 Data Bus 1
P41	3V3	IO CMOS	SDIO_D2	MMC1 Data Bus 2
P42	3V3	IO CMOS	SDIO_D3	MMC1 Data Bus 3

Table 15 MMC pins

5.8 UART: ASYNCHRONOUS SERIAL PORTS

There are three defined UART devices in the module in order to control serial devices or debug via serial. They are available in the SMARC-314 in three blocks of pins.

The IGEP™ SMARC iMX6 uses a 1V8 voltage levels for UART buses. In some cases, voltage translators should be necessary to adapt voltage levels between ICs.

The IGEP™ SMARC iMX6 uses UART2 as a Kernel Debug Peripheral. This UART is an inexpensive method to detect and repair system issues. It is advisable to use another UART instead of UART2 to preserve this functionality. In the next figure is shown how to connect the UART SMARC pins (page 39 of SMARC Design Guide V_IO=1V8).

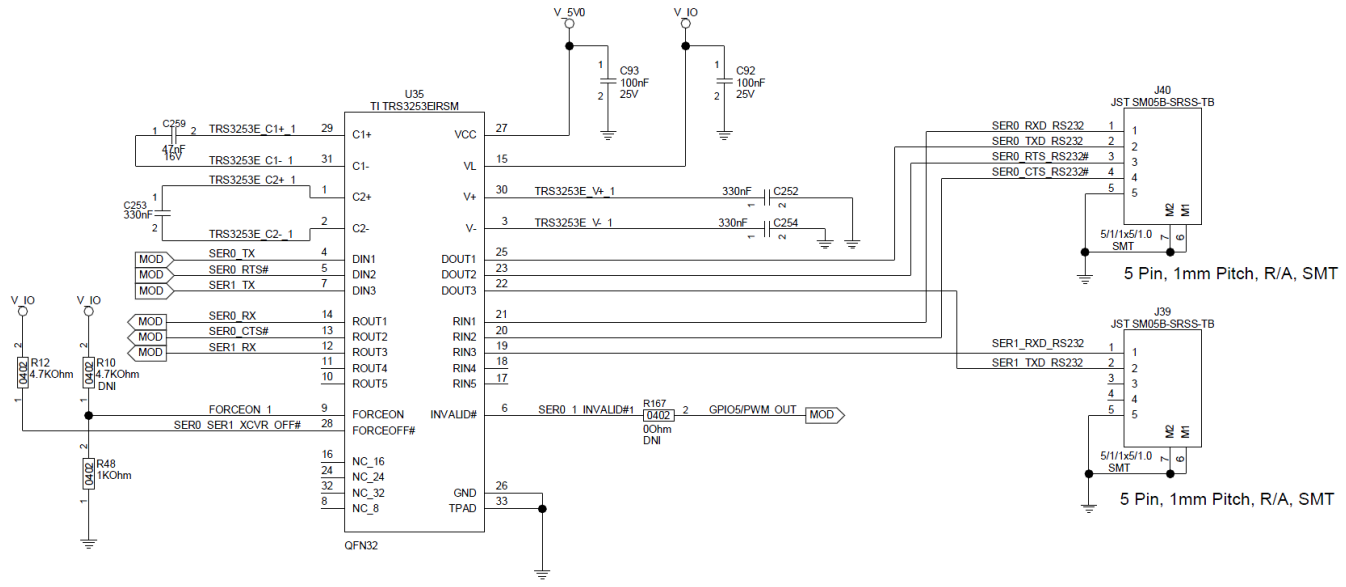

Figure 24 UART SMARC connections

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Pin	Volt Level	Type	Main Function	Comments
1st UART				
P134	1V8	O CMOS	SER1_TX	UART2: Asynchronous serial port 2 data out.
P135	1V8	I CMOS	SER1_RX	UART2: Asynchronous serial port 2 data in.
2nd UART				
P136	1V8	O CMOS	SER2_TX	UART3: Asynchronous serial port 3 data out.
P137	1V8	I CMOS	SER2_RX	UART3: Asynchronous serial port 3 data in.
P138	1V8	O CMOS	SER2_RTS#	UART3: Request to Send handshake line. Active low. CTSn Output
P139	1V8	I CMOS	SER2_CTS#	UART3: Clear to Send handshake line. Active low. RTSn Input
3rd UART				
P140	1V8	O CMOS	SER3_TX	UART4: Asynchronous serial port 4 data out.
P141	1V8	I CMOS	SER3_RX	UART4: Asynchronous serial port 4 data in.

Table 16 UART pins

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5.9 I2S: SERIAL AUDIO PORT

I2S is a synchronous serial bus used for interfacing digital audio devices such as Audio CODECs and DSP chips. Generally PCM audio data is transmitted over the I2S interface. The I2S bus may have a single bidirectional data line or two separate data lines. The signals constituting the I2S bus are a serial clock/ bit clock (output from the master), a left right clock (output from the master) that indicates the channel being transmitted and a single bidirectional data line or two data lines - one input and one output. A SMARC module can generally be configured as I2S master or slave.

In the next example is connected a Stereo CODEC with Headphone AMP to the Serial Audio Port (page 56 of SMARC Design Guide V_IO=1V8).

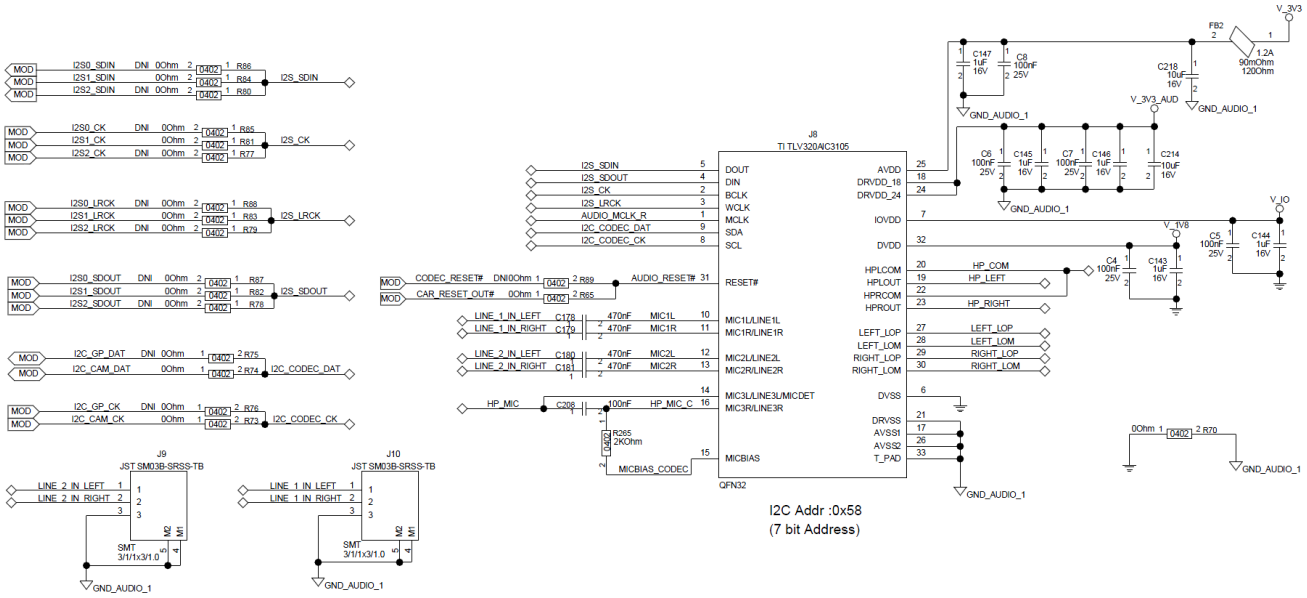

Figure 25 I2S example: Stereo CODEC with Headphone AMP

Pin	Volt Level	Type	Main Function	Comments
S38	1V8	O CMOS	AUDIO_MCK	Master clock output to Audio codecs
S39	1V8	I/O CMOS	I2S0_LRCK	SAI1: iMX6 AUD4 Transmit Frame Sync signal
S40	1V8	O CMOS	I2S0_SDOUT	SAI1: iMX6 AUD4 Data Transmit signal
S41	1V8	I CMOS	I2S0_SDIN	SAI1: iMX6 AUD4 Data Receive signal
S42	1V8	I/O CMOS	I2S0_CK	SAI1: iMX6 AUD4 Transmit Clock signal

Table 17 I2S pins

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5.10 LVDS DISPLAY

The next figure show how to connect LVDS display signals to connector (page 32 of SMARC Design Guide V_IO=1V8).

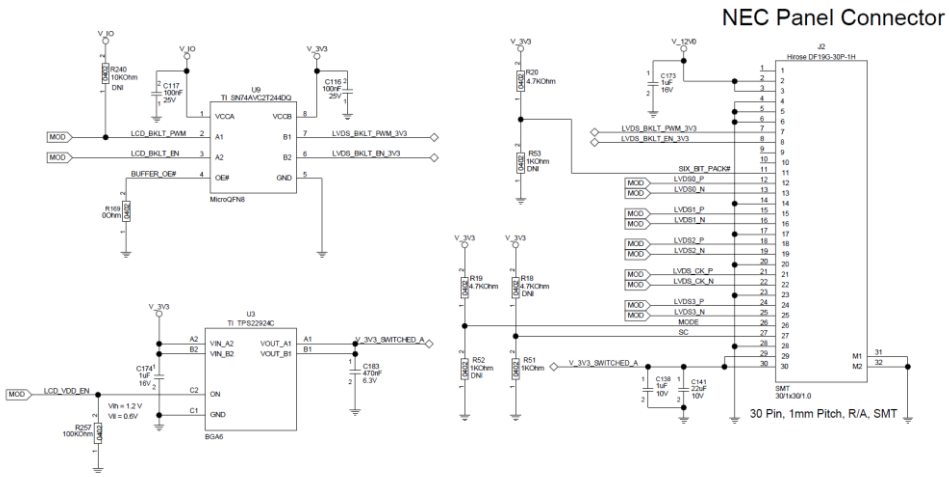

Figure 26 LVDS connection example

Pin	Volt Level	Type	Main Function	Comments
S125	DS	O CMOS	LVDS0+	LVDS data channel differential pair D0 +
S126	DS	O CMOS	LVDS0-	LVDS data channel differential pair D0 -
S128	DS	O CMOS	LVDS1+	LVDS data channel differential pair D1 +
S129	DS	O CMOS	LVDS1-	LVDS data channel differential pair D1 -
S131	DS	O CMOS	LVDS2+	LVDS data channel differential pair D2 +
S132	DS	O CMOS	LVDS2-	LVDS data channel differential pair D2 -
S134	DS	O CMOS	LVDS_CK+	LVDS clock channel differential pair +
S135	DS	O CMOS	LVDS_CK-	LVDS clock channel differential pair -
S137	DS	O CMOS	LVDS3+	LVDS data channel differential pair D3 +
S138	DS	O CMOS	LVDS3-	LVDS data channel differential pair D3 -

Table 18 LVDS pins

5.11 HDMI DISPLAY

The SMARC HDMI data pairs may be routed directly from the SMARC Module pins to a suitable Carrier HDMI connector. Since HDMI is a hot-plug capable interface, it is important for the Carrier to implement ESD protection on all of the HDMI lines. The ESD protection on the data lines must be low capacitance so as not to degrade high speed signalling. The data lines must route through the ESD protection device pins in a no-stub fashion. The ESD protection should be located close to the HDMI connector.

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The next figure show how to connect SMARC HDMI pins to HDMI connector (page 35 of SMARC Design Guide V_IO=1V8).

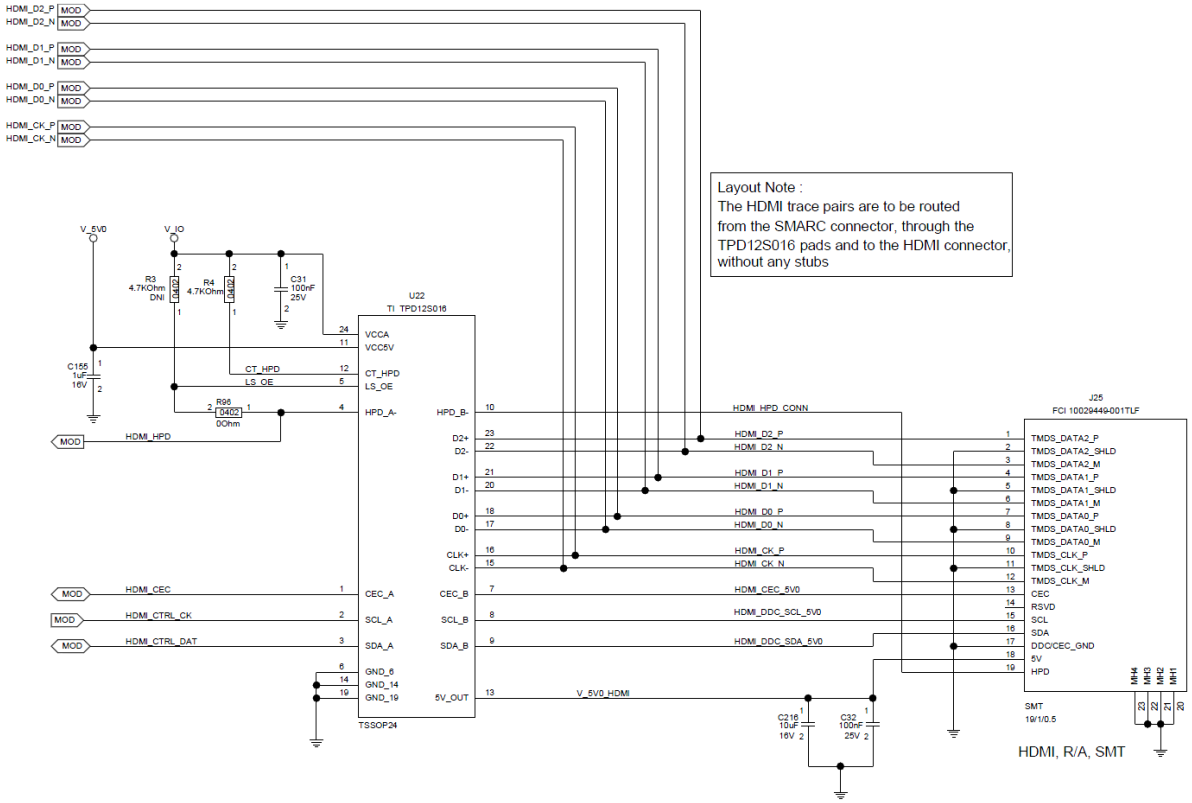

Figure 27 HDMI connection example

Pin	Volt Level	Type	Main Function	Comments
P92	TMDS HDMI	O CMOS	HDMI_D2+	HDMI differential pair data input D2 +
P93	TMDS HDMI	O CMOS	HDMI_D2-	HDMI differential pair data input D2 -
P95	TMDS HDMI	O CMOS	HDMI_D1+	HDMI data differential pair D1 +
P96	TMDS HDMI	O CMOS	HDMI_D1-	HDMI data differential pair D1 -
P98	TMDS HDMI	O CMOS	HDMI_D0+	HDMI data differential pair D0 +
P99	TMDS HDMI	O CMOS	HDMI_D0-	HDMI data differential pair D0 -
P101	TMDS HDMI	O CMOS	HDMI_CK+	HDMI differential clock output pair +
P102	TMDS HDMI	O CMOS	HDMI_CK-	HDMI differential clock output pair -
P104	TMDS HDMI	O CMOS	HDMI_HPD	HDMI Hot Plug Detect input. Active low.
P105	TMDS HDMI	O CMOS	HDMI_CTRL_CK	I2C2 bus clock. Active low.
P106	TMDS HDMI	O CMOS	HDMI_CTRL_DAT	I2C2 bus data. 0x08 is used. Active low.
P107	TMDS HDMI	O CMOS	HDMI_CEC	HDMI Consumer Electronics Control. Active low.

Table 19 HDMI pins

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5.12 MIPI-DSI: DISPLAY SERIAL INTERFACE

The Display Serial Interface (DSI) is a specification by the Mobile Industry Processor Interface (MIPI) Alliance aimed at reducing the cost of display controllers in a mobile device. It is commonly targeted at LCD and similar display technologies. It defines a serial bus and a communication protocol between the host (source of the image data) and the device (destination of the image data).

SMARC does not define MIPI DSI output, but in IGEP™ SMARC iMX6 is connected to S68, S69, S71, S72, S74 and S75 pins as next table show.

Pin	Volt Level	Type	Main Function	Comments
S68	DS	I/O CMOS	AFB_DIFF2+	DSI0: clock differential pair +
S69	DS	I/O CMOS	AFB_DIFF2-	DSI0: clock differential pair -
S71	DS	O CMOS	AFB_DIFF3+	DSI0: data differential pair D0 +
S72	DS	O CMOS	AFB_DIFF3-	DSI0: data differential pair D0 -
S74	DS	O CMOS	AFB_DIFF4+	DSI0: data differential pair D1 +
S75	DS	O CMOS	AFB_DIFF4-	DSI0: data differential pair D1 -
LCD Controls				
S127	1V8	IO	LCD_BKLT_EN	High enables panel backlight
S133	1V8	IO	LCD_VDD_EN	High enables panel VDD
S141	1V8	O CMOS	LCD_BKLT_PWM	Display Backlight. PMW output 4.

Table 20 MIPI-DSI pins

5.13 MIPI-CSI: CAMERA SERIAL INTERFACE

The Camera Serial Interface (CSI) is a specification of the Mobile Industry Processor Interface (MIPI) Alliance. It defines an interface between a camera and a host processor.

There is defined one MIPI-CSI camera serial interface. It support MIPI-CSI 2.0 which main difference is that MIPI-CSI 2.0 uses an I2C bus to communicate with camera (pins I2C_CAM[0:1]).

The next figure shows how to connect MIPI CSI signals to CSI camera (page 81 of SMARC Design Guide), in this example OV3640 is used.

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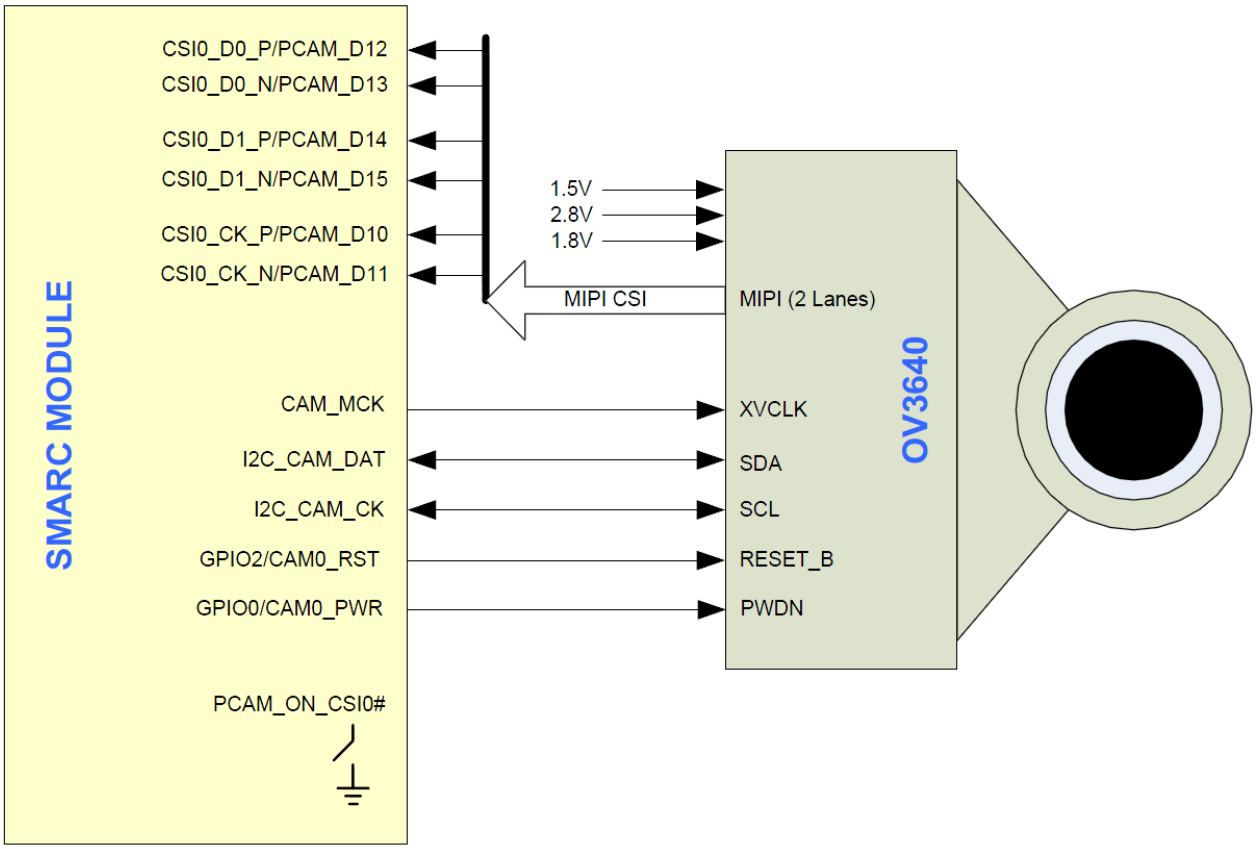

Figure 28 MIPI-CSI connection example

Pin	Volt Level	Type	Main Function	Comments
P3	LVDS D-PHY	I CMOS	CSI1_CK+ / PCAM_D0	CSI1 differential clock input +
P4	LVDS D-PHY	I CMOS	CSI1_CK- / PCAM_D1	CSI1 differential clock input -
P7	LVDS D-PHY	I CMOS	CSI1_D0+ / PCAM_D2	CSI1 differential data input D0 +
P8	LVDS D-PHY	I CMOS	CSI1_D0- / PCAM_D3	CSI1 differential data input D0 -
P10	LVDS D-PHY	I CMOS	CSI1_D1+ / PCAM_D4	CSI1 differential data inputs D1 +
P11	LVDS D-PHY	I CMOS	CSI1_D1- / PCAM_D5	CSI1 differential data inputs D1 -
P13	LVDS D-PHY	I CMOS	CSI1_D2+ / PCAM_D6	CSI1 differential data input D2 +
P14	LVDS D-PHY	I CMOS	CSI1_D2- / PCAM_D7	CSI1 differential data input D2 -
P16	LVDS D-PHY	I CMOS	CSI1_D3+ / PCAM_D8	CSI1 differential data input D3 +
P17	LVDS D-PHY	I CMOS	CSI1_D3- / PCAM_D9	CSI1 differential data input D3 -

Table 21 MIPI-CSI pins

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5.14 SATA

Serial ATA (or SATA) is a high speed point to point serial interface that connects a host system to a mass storage device such as rotating hard drive, solid state drive or an optical drive. Data and clock are serialized onto a single outbound differential pair and a single inbound pair. Data link rates of 1.5, 3.0 and 6.0 Gbps are defined by the SATA specification. A SATA link is AC coupled, but the coupling capacitors are defined in the SMARC specification to be on the Module, for both SATA transmit and receive pairs.

The next figure show how to connect SATA SMARC pins to mSATA connector (page 77 of SMARC Design Guide).

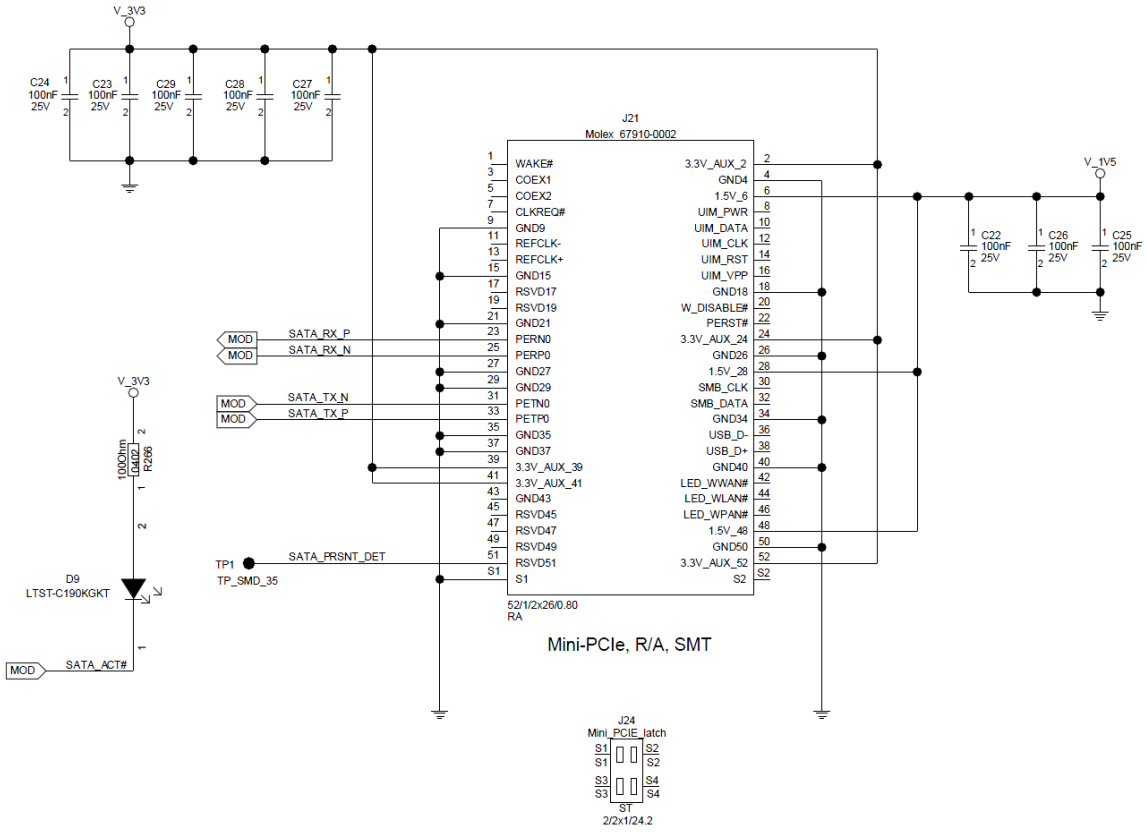

Figure 29 SATA connection example

Pin	Volt Level	Type	Main Function	Comments
P48	DS	SATA 3 Gb/s	SATA_TX+	Differential SATA transmit data +. This signal has a 10 nF coupling capacitor.
P49	DS	SATA 3 Gb/s	SATA_TX-	Differential SATA transmit data -. This signal has a 10 nF coupling capacitor.
P51	DS	SATA 3 Gb/s	SATA_RX+	Differential SATA receive data +. This signal has a 10 nF coupling capacitor.
P52	DS	SATA 3 Gb/s	SATA_RX-	Differential SATA receive data -. This signal has a 10 nF coupling capacitor.
S54	3V3	O CMOS	SATA_ACT#	Active low SATA activity indicator

Table 22 SATA pins

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5.15 PCIe: PCI EXPRESS

PCI Express (or PCIe) is a scalable, point-to-point serial bus interface commonly used for high speed data exchange between a PCIe host, or root, and a target device. It is scalable in the sense that there may be link widths, per the PCIe specification, that are x1, x2, x4, x8, x16 or x32. SMARC currently calls out only x1 operation. A PCIe link is AC coupled, but the coupling capacitors are defined in the SMARC specification to be on the Module, for only PCIe transmit pair.

The next figure show how to connect PCIe SMARC pins to Mini-PCIe connector (page 75 of SMARC Design Guide).

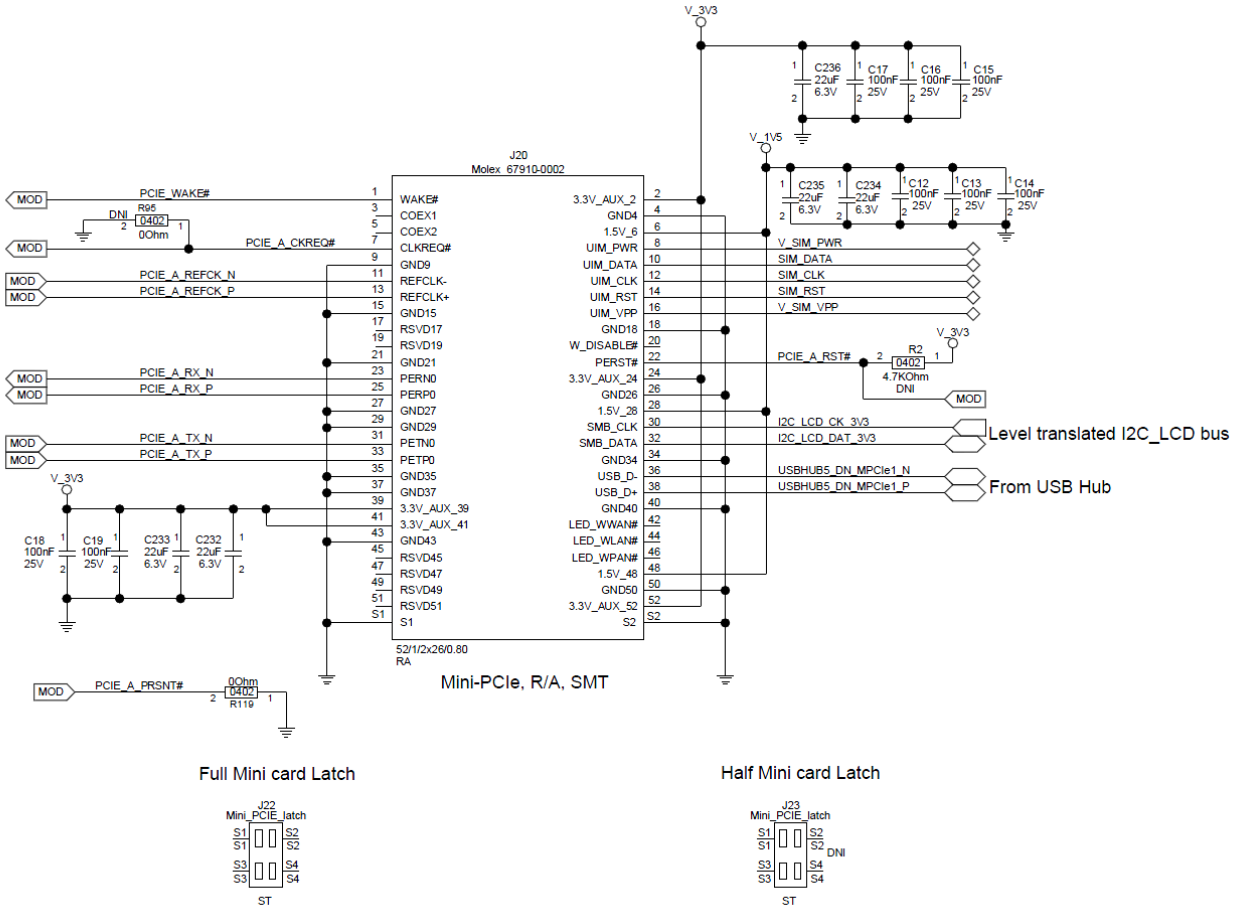

Figure 30 PCIe connection example

Pin	Volt Level	Type	Main Function	Comments
P74	3V3	I CMOS	PCIE_A_PRSNT#	PCIe Port A: Hotplug presence detect. Active low. Active low
P75	3V3	O CMOS	PCIE_A_RST#	PCIe Port A: Port reset output. Active low.
P78	3V3	I CMOS	PCIE_A_CKREQ#	PCIe Port A: clock request input. Active low
P83	LVDS PCIe	O CMOS	PCIE_A_REFCK+	PCIeA: Differential PCIe Link A reference clock output DC coupled.
P84	LVDS PCIe	O CMOS	PCIE_A_REFCK-	PCIeA: Differential PCIe Link A reference clock output DC coupled.

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P86	LVDS PCIe	I CMOS	PCIE_A_RX+	PCIeA: Differential PCIe Link A receive data pair 0.
P87	LVDS PCIe	I CMOS	PCIE_A_RX-	PCIeA: Differential PCIe Link A receive data pair 0.
P89	LVDS PCIe	O CMOS	PCIE_A_TX+	PCIeA: Differential PCIe Link A transmit data pair 0. This signal has a 0.1 uF coupling capacitor.
P90	LVDS PCIe	O CMOS	PCIE_A_TX-	PCIeA: Differential PCIe Link A transmit data pair 0. This signal has a 0.1 uF coupling capacitor.

Table 23 PCI3 pins

5.16 CAN BUS: CONTROLLER AREA NETWORK

The SMARC iMX6 can be integrated in a global system using the serial standard CAN bus. The CAN bus is a standard designed to allow microcontrollers and devices to communicate with each other without a host computer. It is a differential half duplex data bus, using shielded or unshielded twisted pair wiring, with an impedance termination of 120 W at the endpoint of the bus. Nodes on the bus are arranged in daisy-chain fashion.

A CAN Transceiver is needed on the baseboard to connect the system to the CAN Bus. In the next example (page 61 of SMARC Design Guide V_IO=1V8), are showing this application using the NCV7341 chip (it's a high-speed CAN Transceiver).

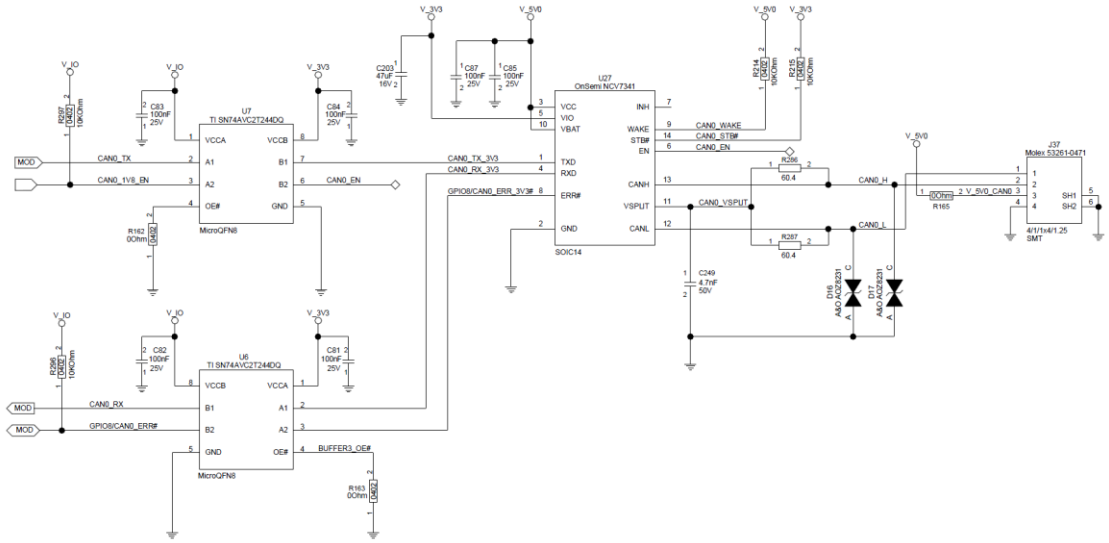

Figure 31 CAN Bus circuit example

Pin	Volt Level	Type	Main Function	Comments
P143	1V8	O CMOS	CAN0_TX	CAN1 Transmission line
P144	1V8	I CMOS	CAN0_RX	CAN1 Reception line
P145	1V8	O CMOS	CAN1_TX	CAN2 Transmission line
P146	1V8	I CMOS	CAN1_RX	CAN2 Reception line

Table 24 CAN pins

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5.17 GPIO: GENERAL PURPOSE INPUT OUTPUT

GPIOs are input/output (IO) general purpose pins used to control LEDs, relays, switch, etc. In the next figure is shown a basic circuit with an input pushbutton and two outputs to manage LED signals.

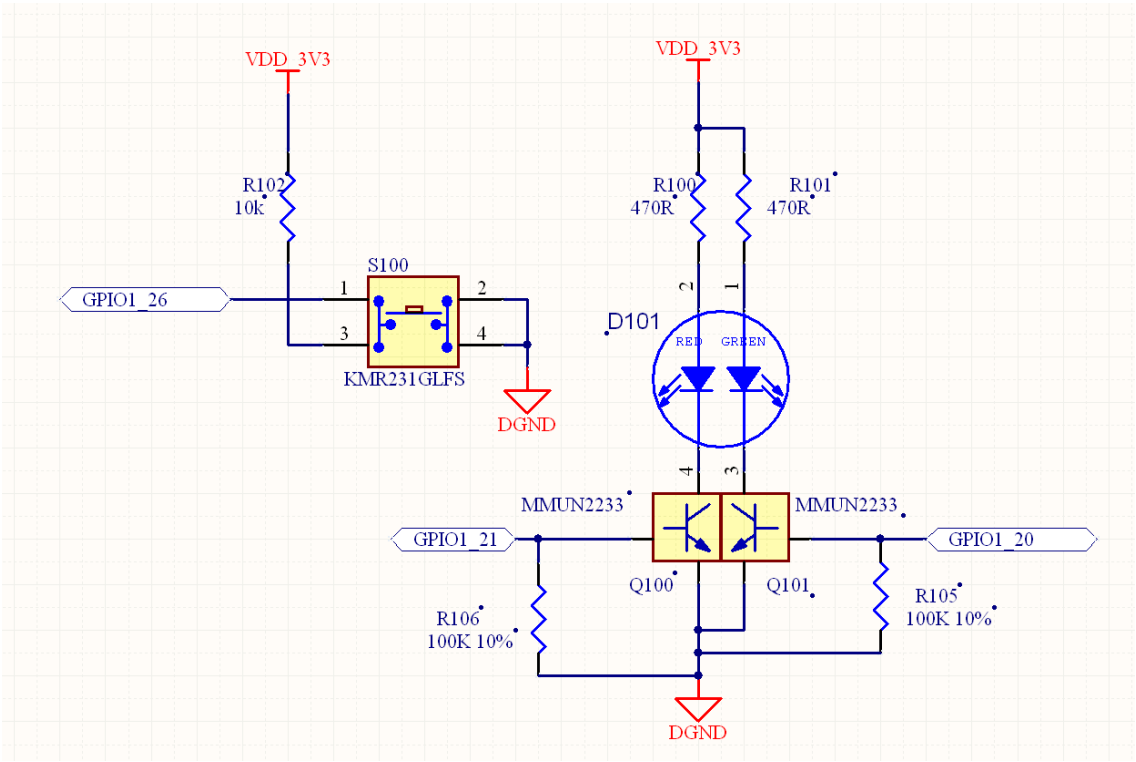

Figure 32 GPIOs example: control circuit to manage LEDs

Pin	Volt Level	Type	Main Function	Comments
P108	1V8	IO CMOS	GPIO0 / CAM0_PWR#	General purpose input/output
P109	1V8	IO CMOS	GPIO1 / CAM1_PWR#	General purpose input/output
P110	1V8	IO CMOS	GPIO2 / CAM0_RST#	General purpose input/output
P111	1V8	IO CMOS	GPIO3 / CAM1_RST#	General purpose input/output
P112	1V8	IO CMOS	GPIO4 / HDA_RST#	General purpose input/output
P113	1V8	IO CMOS	GPIO5 / PWM_OUT	PMW Output 1 or General purpose input/output
P114	1V8	IO CMOS	GPIO6 / TACHIN	General purpose input/output
P115	1V8	IO CMOS	GPIO7 / PCAM_FLD	General purpose input/output
P116	1V8	IO CMOS	GPIO8 / CAN0_ERR#	General purpose input/output
P117	1V8	IO CMOS	GPIO9 / CAN1_ERR#	General purpose input/output
P118	1V8	IO CMOS	GPIO10	General purpose input/output
P119	1V8	IO CMOS	GPIO11	General purpose input/output

Table 25 GPIO pins.

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5.18 PWM: PULSE-WIDTH MODULATION

If it is needed a control over other devices via a Pulse-Width Modulation (PWM), the module offers a PWM peripheral with 16 bits time-base with Period and Frequency control and two outputs.

Max PWM frequency is 66 MHz. More information at chapter 52 from iMX6 Applications Processor Reference Manual.

In the next figure is shown a simple example in which the PWM signal is sent to a RC-filter.

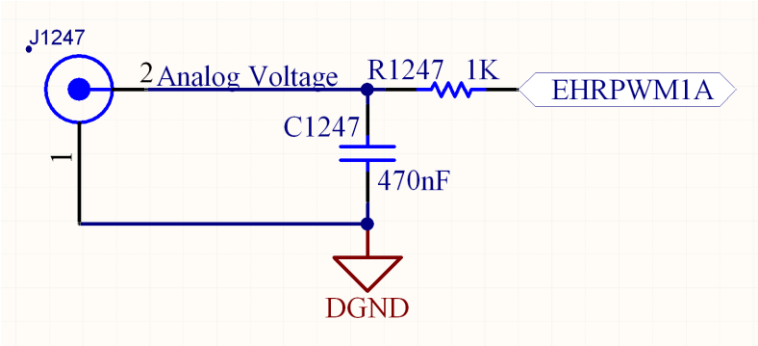

Figure 33 PWM example: RC filter

Pin	Volt Level	Type	Main Function	Comments
P113	1V8	IO CMOS	GPIO5 / PWM_OUT	PMW Output 1 or General purpose input/output
S18	1V8	O CMOS	AFB1_OUT	PWM output 3
S141	1V8	O CMOS	LCD_BKLT_PWM	Display Backlight. PMW output 4.

Table 26 PWM pins

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5.19 RTC BATTERY

The RTC Battery pin (S147) allows the connection of a battery. With this, in case of a general power fall, RTC circuit will be powered. The user has to be careful with the selection of battery capacity: depending on the current consumption, the activity duration will be drastically reduced.

Next figure shows RTC Battery examples (page 30 of SMARC Design Guide).

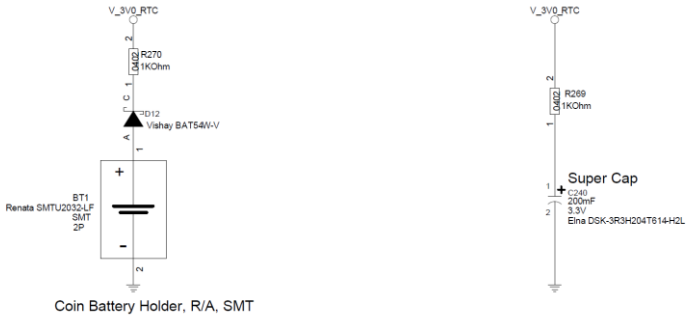

Figure 34 RTC Battery

The Carrier Board must be implemented the needed circuits to protect against charging by reverse currents.

Pin	Volt Level	Type	Main Function	Comments
S147	3V0	Power	VDD_RTC	Low current RTC circuit backup power – 3.0V nominal. May be sourced from a Carrier based lithium cell or super cap.

Table 27 RTC Battery pin

5.20 ENVIRONMENTAL SPECIFICATION

General Specification	Operating	Non-operating
Industrial grade (E2)	-40ºC to +80ºC	-40ºC to +80ºC

Table 28 Temperature range

Standard modules are available for Industrial grade temperature range. The operating temperature is the maximum measurable temperature on any spot on the module's surface.

- **Humidity**

93% relative Humidity at 40ºC, non-condensing (according to IEC 60068-2-78).

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5.21 STANDARDS AND CERTIFICATIONS

- **RoHS**

The SMARC iMX6 is compliant to the directive 2002/95/EC on the restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment.

- **CE Marking**

The SMARC iMX6 is CE marked according to Low Voltage Directive 2006/95/EC – Test standard EN60950.

- **WEEE Directive**

WEEE Directive 2002/96/EC is not applicable for Computer-on-Modules.

- **Conformal Coating**

Conformal Coating is available for Computer-on-Modules and for validated SMARC modules. Please, contact your local sales or support for further details.

- **EMC**

The SMARC iMX6 is designed and tested following EN55022 standard (“INFORMATION TECHNOLOGY EQUIPMENT. RADIO DISTURBANCE CHARACTERISTICS. LIMITS AND METHODS OF MEASUREMENT”).

- **SMARC Form Factor standard**

The SMARC (“Smart Mobility Architecture”) is a versatile small form factor computer Module definition targeting application that require low power, low costs and high performance.

5.22 MTBF

The SMARC iMX6 has been designed with a predicted MTBF (Mean Time Before Failure) of >131400 hours (>15 years).

All hardware components are selected with long time industrial reliability parameters. The MTBF prediction of hardware components and temperature stress could be estimated, but the newest devices are very software dependent. So, final application has an important effect on MTBF.

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5.23 MECHANICAL SPECIFICATION

- **Module Dimension**

82,00 mm x 50,00 mm x 4,30 mm (high without JTAG connector)

- **Mechanical Drawing**

The next figures show the SMARC iMX6 modules mechanical dimensions:

- All dimensions are in millimeters.
- 8-layer Printed Circuit Board size is 82,00 mm x 50,00 mm x 1,15 mm.
- Mounting holes are provided, one on each corner.

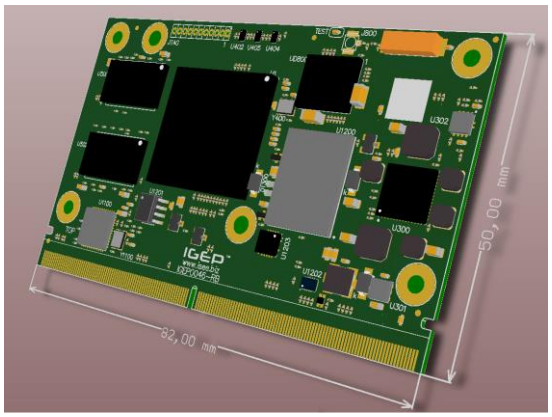

Figure 35 IGEP™ SMARC iMX6 Main Outline Dimensions

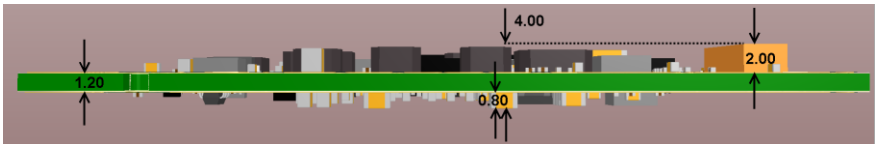

Figure 36 IGEP™ SMARC iMX6 Lateral view Widths Dimensions

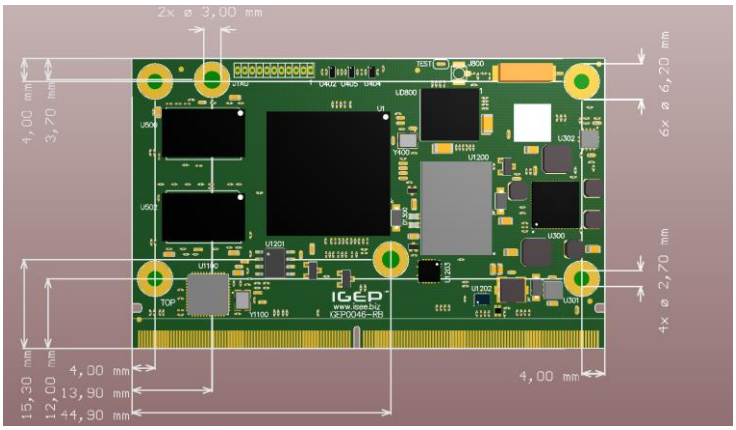

Figure 37 IGEP™ SMARC iMX6 side view detailed mechanical dimensions

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6 ON-BOARD INTERFACES

6.1 SUMMARY

Device	Connector	Reference	Description
LEDs	-	D1300 and D1301	GPIO controlled
JTAG	11-pin 1,25 mm pitch interface	JTAG	-

Table 29 Interface summary

6.2 LEDs

The IGEP™ SMARC iMX6 module provides two bicolor LED indicator on the board. They can be controlled by the user through GPIOs.

Signal Name	LED Color	Description
DI0_PIN2	D1300 Red	DI0_PIN2 of iMX6
DI0_PIN3	D1300 Green	DI0_PIN3of iMX6
DI0_PIN4	D1301 Red	DI0_PIN4 of iMX6
DI0_PIN15	D1301 Green	DI0_PIN15 of iMX6

Table 30 LEDs

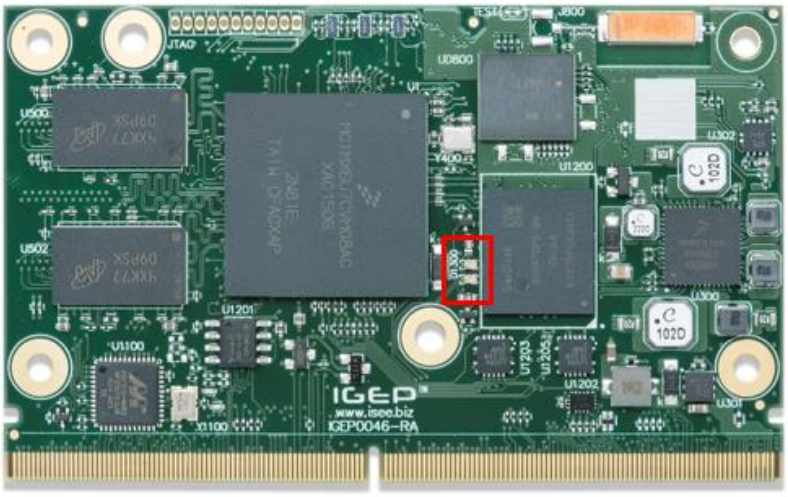

Figure 38 LEDs position in the PCB

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6.3 JTAG

The SMARC iMX6 provides a footprint JTAG interface to help in the developing of user's code.

The JTAG port is designed to support features compatible with the IEEE standard 1149.1 v2001 (JTAG). Support IEEE P1149.6 extensions to the JTAG standard are for AC testing of selected IO signals.

The JTAG port allows debug-related control and status, such as putting selected cores into reset and/or debug mode and the ability to monitor individual core status signals via JTAG.

Figure 39 JTAG position in the PCB

Next figure shows the pinout schematic and the corresponding metal contacts.

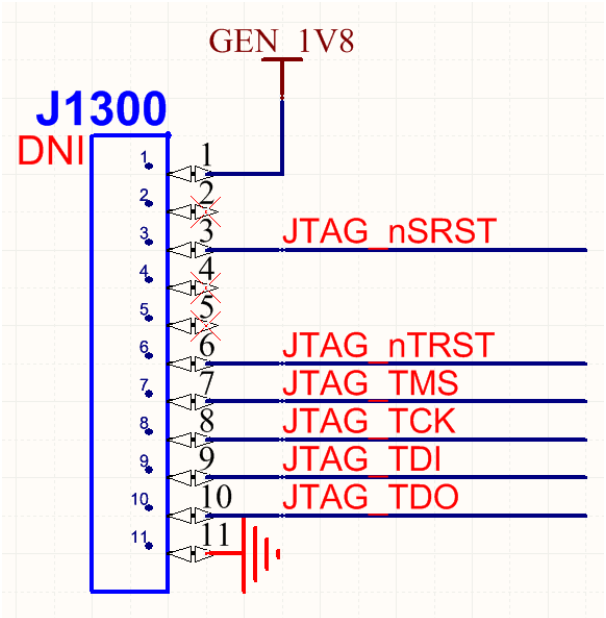

Figure 40 JTAG connector schematic

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Note that even pins are left unconnected but the footprint makes possible to use a 11 pin 1.27 mm pitch connector. The next table details the signals on each pin of J1300.

Signal Name	JTAG pin	Description
GEN_1V8	1	1.8V Supply
NC	2	Not Connected
JTAG_nSRST	3	System Reset Input Signal
NC	4	Not connected
NC	5	Not connected
JTAG_nTRST	6	JTAG Test Reset Input Signal
JTAG_TMS	7	JTAG Test Mode Select Input Signal
JTAG_TCK	8	JTAG Test Clock Input Signal
JTAG_TDI	9	JTAG Test Data Input Signal
JTAG_TDO	10	JTAG Test Data Output Signal
GND	11	Ground

Table 31 JTAG pinout

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7 ELECTRICAL CHARACTERISTICS

Electrical parameter	Min	Typ	Max	Unit
5 V INPUT POWER SUPPLY				
SMARC iMX6 DC Input Power Supply Voltage	2.5	5	5.5	V
SMARC iMX6 DC Input Power Supply Current (1)	-	0.32	2	A
Input/Output pins (2)				
Output High-Level DC Voltage	1.65	-	1.8	V
Input High-Level DC Voltage	1.26	-	1.8	V
Output Low-Level DC Voltage	-	-	0.15	V
Input Low-Level DC Voltage	0	-	0.54	V
RTC_BATTERY type pins				
Input DC Voltage	2.5	3	3.25	V

Table 32 IGEP™ SMARC iMX6 Electrical Characteristics

(1) Current measured with default delivered software. Be aware that different software configurations could drastically modify current consumption.

(2) The electrical specification depends on the configured mode. For accurate information of each pin, revise iMX6 Applications Processor official document from NXP official site https://www.nxp.com/

SMARC iMX6 MODULES CAN BE DAMAGED IF ANY OF THESE ELECTRICAL LIMITS ARE EXCEEDED AND/OR ELECTROSTATIC DISCHARGE PRECAUTIONS ARE NOT FOLLOWED.

WARRANTY LOST IF IMPROPER USE OF THE MODULE IS FOUND.

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8 EXPANSION BOARD

All the products in the SMARC iMX6 series can be supplemented with next expansion board.

Part Number	IGEP™ Device	Description
BASE0040-DFEV-UGAC	BASE SMARC EXPANSION	Designed for fast prototyping of user's projects

The BASE SMARC EXPANSION is a fully equipped baseboard that access to almost all SMARC functionalities. It has been designed to be used as the fastest way to develop and check the user's final application before building a prototype, saving costs and reducing time to market.

This model can be used with all the ISEE ASSEMBLY TECHNOLOGY's SMARC series modules. Thanks to this design, the user only needs to purchase one Expansion board to check all SMARC modules manufactured by ISEE ASSEMBLY TECHNOLOGY.

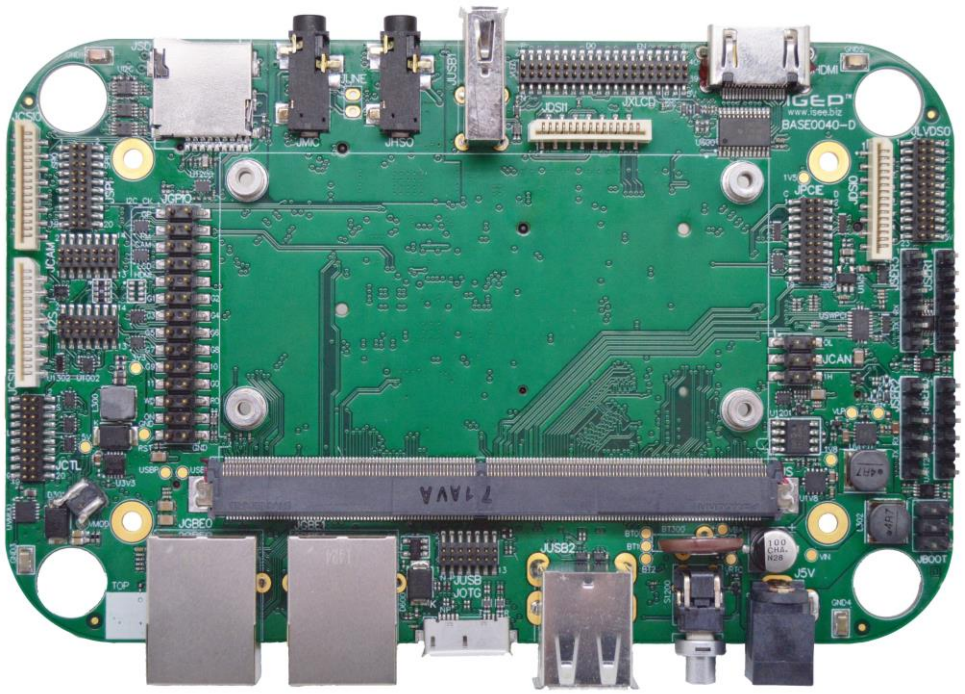

Figure 41 BASE0040 SMARC EXPANSION Rev. D

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The following table contains all the features and capabilities of the BASE SMARC EXPANSION.

Connectors	Features	Dimensions	Case Dimensions
1 x SMARC connector 1 x Power Supply (+5 V) connector 2 x 10/100/1000 Mbps Base RJ45 1 x HDMI Type A receptacle 1 x LCD 24-bit connector 1 x Touchscreen connector 1 x XLCD expansion 40-pin header 1 x LVDS expansion 24-pin header 2 x CSI connector, 2-lanes 1 x Parallel Camera expansion 14-pin header 1 x Stereo Line Input Mic/Line 1 x Stereo Line Output Headphone 1 x I2S 14-pin header 3 x USB 2.0 Type A receptacle 1 x USB 3.0 Type AB receptacle 1 x USB2 expansion 14-pìn header 1 x Modem USB & PCIe interface 1 x mSATA & PCIe interface 1 x PCI expansion 20-pin header 1 x Micro-SD connector 1 x SIM-card connector 2 x DSI connector 2 x CAN on a 6-pin header 1 x SPI 20-pin header 1 x I/O expansion 28-pin header 4 x Serial UART 3V3 expansion 6-pin header	1 x Button-LED (2 LEDs: red, blue) 3 x Boot jumpers 1 x Control 20-pin header	142,00 mm x 90,00 mm (without case)	150,00 mm x 100,00 mm x 30,00 mm

Table 33 BASE0040 SMARC EXPANSION Features Rev. D

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9 DOCUMENT AND STANDARDS REFERENCES

- **CAN** (“Controller Area Network”) Bus Standards
  ISO 11898-1:2015 Road vehicles - Controller area network (CAN) - Part 1: Data link layer and physical signaling, (https://www.iso.org)
  ISO 11992-1:2019 Road vehicles - Interchange of digital information on electrical connections between towing and towed vehicles - Part 1: Physical and data-link layers (https://www.iso.org)
  SAE J2411: Feb 14, 2000, Single Wire CAN Network for Vehicle Applications (https://www.sae.org)
- **MIPI CSI-2** (Camera Serial Interface version 2) The MIPI CSI-2 standard is owned and maintained by the MIPI Alliance (“Mobile Industry Processor Alliance”) (www.mipi.org)
- **MIPI CSI-3** (Camera Serial Interface version 3) The MIPI CSI-3 standard is owned and maintained by the MIPI Alliance (“Mobile Industry Processor Alliance”) (www.mipi.org)
- **COM Express** – the formal title for the COM Express specification is “PICMG® COM.0 COM Express Module Base Specification”, Revision 3.0, March 31, 2017. This standard is owned and maintained by the PICMG (“PCI Industrial Computer Manufacturer’s Group”) (www.picmg.org)
- **DisplayPort and Embedded DisplayPort -** These standards are owned and maintained by VESA (“Video Electronics Standards Association”) (www.vesa.org)
- **MIPI DSI** (Display Serial Interface) The DSI standard is owned and maintained by the MIPI Alliance (“Mobile Industry Processor Alliance”) (www.mipi.org)
- **eMMC** (“Embedded Multi-Media Card”) The eMMC electrical standard is defined by JEDEC JESD84-B51A and the mechanical standard by JESD84-C44 (www.jedec.org)
- **eSPI** (“Enhanced Serial Peripheral Interface”) The eSPI Interface Base Specification is defined by Intel (https://www.intel.com)
- **Fieldbus** - this term refers to a number of network protocols used for real – time industrial control. Refer to the following web sites: https://www.profibus.com/download/ and www.can-cia.org
- **GBE MDI** (“Gigabit Ethernet Medium Dependent Interface”) This is defined by IEEE 802.3. The 1000Base-T operation over copper twisted pair cabling is defined by IEEE 802.3ab (www.ieee.org)
- **HDA (HD Audio),** High Definition Audio Specification, Intel, Revision 1.0a, June 17, 2010 (http://www.intel.com)
- **HDMI Specification,** Version 2.1, November 28, 2017 (www.hdmi.org)
- **I2C Specification,** Version 6.0, April 4th 2014, Philips Semiconductor (now NXP) (www.nxp.com)
- **I2S Bus Specification**, Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) (www.nxp.com)
- **IEEE1588 - 2008**. IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems (http://standards.ieee.org)
- **JTAG** (“Joint Test Action Group”) This is defined by IEEE 1149.1-2001 - IEEE Standard Test Access Port and Boundary Scan Architecture (https://ieeexplore.ieee.org)
- **MXM3** Graphics Module Mobile PCI Express Module Electromechanical Specification, Version 3.1, NVidia Corporation
- **PICMG® EEEP** Embedded EEPROM Specification, Rev. 1.0, August 2010 (www.picmg.org)
- **PCI Express** Specifications (www.pci-sig.org)
- **Serial ATA** Revision 3.1, July 18, 2011, Gold Revision, © Serial ATA International Organization (www.sata-io.org) SMARC 2.1.1 Specification © 2020 SGET e.V. Page 9 of 109
- **SD Specifications** Part 1 Physical Layer Simplified Specification, Version 6.00, Aug 29, 2018, SD Group and SD Card Association (“Secure Digital”) (www.sdcard.org)

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- **SM Bus** – “System Management Bus” Specification Version 3.1, March 19, 2018, System Management Interface Forum, Inc. (http://www.smbus.org)
- **SPI Bus** – “Serial Peripheral Interface” – de-facto serial interface standard defined by Motorola. A good description may be found on Wikipedia (http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus)
- **USB** Specifications (http://www.usb.org)

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