Smart Mobility ARChitecture

Hardware Specification

Version 2.0 June 2nd, 2016

STANDARDIZATION
GROUP FOR
EMBEDDED
TECHNOLOGIES

1 INTRODUCTION

1.1 Legal

1.2 Revision History

Rev	Date	Originator	Notes
1.0	Dec. 20, 2012	S. Milnor	Initial release
1.1	May 29, 2014	S. Milnor	Change notes for V1.0 to V1.1 can be found in the V1.1 document
2.0		C. Eder	See section 10.1 ‘SMARC HW Specification Changes V1.1 to V2.0’ on page 72

1.3 Table of Contents

1.4 Table of Figures

1.5 General Introduction

The SMARC ("Smart Mobility ARChitecture") is a versatile small form factor computer Module definition targeting applications that require low power, low costs, and high performance. The Modules will typically use ARM SOCs similar or the same as those used in many familiar devices such as tablet computers and smart phones. Alternative low power SOCs and CPUs, such as tablet oriented X86 devices and other RISC CPUs ***may*** be used as well. The Module power envelope is typically under 6W although designs up to about 15W are possible.

Two Module sizes are defined: 82mm x 50mm and 82mm x 80mm. The Module PCBs have 314 edge fingers that mate with a low profile 314 pin 0.5mm pitch right angle connector (the connector is sometimes identified as a 321 pin connector, but 7 pins are lost to the key).

The Modules are used as building blocks for portable and stationary embedded systems. The core CPU and support circuits, including DRAM, boot flash, power sequencing, CPU power supplies, GBE and dual channel LVDS display transmitter are concentrated on the Module. The Modules are used with application specific Carrier Boards that implement other features such as audio CODECs, touch controllers, wireless devices, etc. The modular approach allows scalability, fast time to market and upgradability while still maintaining low costs, low power and small physical size.

1.6 Purpose of This Document

This document defines the Module mechanical, electrical, signal and thermal parameters at a level of detail sufficient to provide a framework for SMARC Module and Carrier Board designs.

1.7 Document and Standards References

- ***BT.656*** ("Recommendation ITU-R BT.656-5 Interface for digital component video signals in 525-line and 625-line television systems operating at the 4:2:2 level of Recommendation ITU-R BT.601"), International Telecommunications Union, December 2007 (**www.itu.int**)
- ***CAN*** ("Controller Area Network") Bus Standards – ISO 11898, ISO 11992, SAE J2411
- ***CSI-2*** (Camera Serial Interface version 2) The CSI-2 standard is owned and maintained by the MIPI Alliance ("Mobile Industry Processor Alliance") (**www.mipi.org**)
- ***CSI-3*** (Camera Serial Interface version 3) The CSI-2 standard is owned and maintained by the MIPI Alliance ("Mobile Industry Processor Alliance") (**www.mipi.org**)
- ***COM Express*** – the formal title for the COM Express specification is "PICMG® COM.0 COM Express Module Base Specification", Revision 2.1, May 14, 2012. This standard is owned and maintained by the PICMG ("PCI Industrial Computer Manufacturer's Group") (**www.picmg.org**)
- ***DisplayPort and Embedded DisplayPort*** These standards are owned and maintained by VESA ("Video Electronics Standards Association") (**www.vesa.org**)
- ***D-PHY CSI-2 physical layer standard*** – owned and maintained by the MIPI Alliance (**www.mipi.org**)
- ***DSI*** (Display Serial Interface) The DSI standard is owned and maintained by the MIPI Alliance ("Mobile Industry Processor Alliance") (**www.mipi.org**)
- ***eMMC*** ("Embedded Multi-Media Card") The eMMC electrical standard is defined by JEDEC JESD84-B45 and the mechanical standard by JESD84-C44 (**www.jedec.org**)
- ***eSPI*** ("Enhanced Serial Peripheral Interface") The eSPI Interface Base Specification is defined by Intel (**https://downloadcenter.intel.com/de/download/22112**)
- ***Fieldbus*** - this term refers to a number of network protocols used for real – time industrial control. Refer to the following web sites: **www.profibus.com/downloads** and **www.canopen.org**
- ***GBE MDI*** ("Gigabit Ethernet Medium Dependent Interface") This is defined by IEEE 802.3. The 1000Base-T operation over copper twisted pair cabling is defined by IEEE 802.3ab (**www.ieee.org**)
- ***HDA (HD Audio)***, High Definition Audio Specification, Intel, Revision 1.0a, June 17, 2010 (**http://www.intel.com/content/dam/www/public/us/en/documents/product-specifications/high-definition-audio-specification.pdf**)
- ***HDMI Specification***, Version 1.3a, November 10, 2006 © 2006 Hitachi and other companies (**www.hdmi.org**)
- ***I2C Specification***, Version 2.1, January 2000, Philips Semiconductor (now NXP) (**www.nxp.com**)
- ***I2S Bus Specification***, Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) ()
- ***IEEE1588 - 2008***. IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems (***http://standards.ieee.org/findstds/standard/1588-2008.html***)
- ***JTAG*** ("Joint Test Action Group") This is defined by IEEE 1149.1-2001 - IEEE Standard Test Access Port and Boundary Scan Architecture (www.ieee.org)
- ***MXM3*** Graphics Module Mobile PCI Express Module Electromechanical Specification, Version 3.0, Revision 1.1, © 2009 NVidia Corporation (**www.mxm-sig.org**)
- ***PICMG® EEEP*** Embedded EEPROM Specification, Rev. 1.0, August 2010 (**www.picmg.org**)
- ***PCI Express*** Specifications (**www.pci-sig.org**)
- ***Serial ATA*** Revision 3.1, July 18, 2011, Gold Revision, © Serial ATA International Organization (**www.sata-io.org**)
- ***SD Specifications*** Part 1 Physical Layer Simplified Specification, Version 3.01, ***May*** 18, 2010, © 2010 SD Group and SD Card Association ("Secure Digital") (**www.sdcard.org**)

- ***SM Bus*** – “System Management Bus” Specification Version 3.0, 2© 2014 System Management Interface Forum, Inc. (**http://www.smbus.org**)
- ***SPI Bus*** – “Serial Peripheral Interface” – de-facto serial interface standard defined by Motorola. A good description may be found on Wikipedia (**http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus**)
- ***USB*** Specifications (**www.usb.org**)

2 MODULE OVERVIEW

2.1 Form Factor Feature Summary

- Small form factor, low profile and low power edge-finger card format Module with pin-out optimized for ARM and x86 architecture processors; may also be used with low power, tablet oriented X86 and RISC devices.
- Two Module sizes:
  - 82mm x 50mm
  - 82mm x 80mm
- Carrier Board connector: 314 pin 0.5mm pitch R/A memory socket style connector
  - Originally defined for use with MXM3 graphics cards
  - SMARC Module pin-out is separate from and not related to MXM3 pin-out
  - Multiple sources for Carrier Board connector
  - Low cost
  - Low profile:
    - As low as 1.5mm (Carrier Board top to Module bottom)
    - Other stack height options available, including 2.7mm, 5mm, 8mm
    - Overall assembly height (Carrier Board top to tallest Module component) is less than 6mm
  - Excellent signal integrity – suitable for 2.5 GHz / 5 GHz / 8 GHz data rate signals such as PCIe Gen 1, Gen 2 and Gen 3.
  - Robust, vibration resistant connector
- Module input voltage range: 3.0V to 5.25V
  - Allows operation from 3.6V nominal Lithium-ion battery packs
  - Allows operation from 3.3V fixed DC supply
  - Allows operation from 5.0V fixed DC supply
  - Single supply (no separate standby voltage)
  - Module power pins allow 5A max, or 15W max input power at 3.0V
- Low power designs
  - 2 to 6W typical Module power draw during active operation
  - Fanless
  - Passive cooling
  - Low standby power
  - Design for battery operation
  - 1.8V default I/O voltage

2.2 Module Interface Summary

The interfaces listed below are available per the Module pin definition. Some features are optional and availability is Module design dependent.

- Display Interfaces
  - Single or dual channel LVDS LCD 18 or 24 bit (usually derived from SOC parallel LCD data)
    - Panel support signals (I2C, Power Enables, PWM)
    - Support for dual channel implementations
    - Multiplexing with eDP and MIPI DSI
  - HDMI port multiplexed with DP++ full featured implementation

    - Additional full featured DisplayPort++
- Camera Interfaces
    - Serial configuration: MIPI CSI (2 lane) + MIPI CSI (2 or 4 lane)
- SDIO Interface
    - 4 bit SDIO card interface with support lines
- SPI Interfaces
    - Two SPI interfaces
        - One maybe implemented as eSPI (x86) or QSPI (ARM)
- Audio Interfaces
    - One I2S interface
    - One HDA interfaced multiplexed with second I2S interface
        -
- I2C Interfaces
    - Five I2C interfaces
        - Power Management
        - General Purpose
        - Camera 2 interfaces
        - LCD Display ID
    - HDMI interface also has private I2C interface for HDMI use
- Asynchronous Serial Port Interfaces
    - Four asynchronous serial ports
        - Two with 2 wire handshake (RXD, TXD, RTS#, CTS#)
        - Two with data only (RXD, TXD)
        - Logic level interface
- CAN Bus Interfaces
    - Two CAN bus interfaces
        - Logic level signals from Module based CAN bus protocol controllers
        - RXD, TXD only
- USB Interfaces
    - Six ports total
    - Two sets of super speed signals for support of two USB 3.0 ports
    - Two ports allows USB OTG (USB client or host)
    - USB support signals (VBUS enable / Over-current detects, OTG support signals)
- PCI Express
    - Four PCIe lanes
    - PCIe Gen1, Gen 2 or Gen 3 (Module dependent)
    - Three reference clock pairs
    - Three PCIe reset signals
    - Common PCIe wake signal (PCIE_WAKE#)
- SATA Interface
    - One SATA interface
    - Gen 1, 2 or 3 (Module dependent)
- Gigabit Ethernet
    - Two analog GBE MDI interface
    - No magnetics on Module
    - LED support signals

    - CTREF (center tap reference voltage) for Carrier magnetics (if required by the Module GBE PHY)
    - Individual IEEE1588 trigger signal for each Ethernet interface to allow for enhanced real time applications. This utilizes a software definable pin (SDP) from the Ethernet controller.
- Watchdog Timer Interface
- General Purpose I/O
    - Twelve GPIO signals
    - Specific alternate functions are assigned to some GPIOs
        - PWM / Tachometer capability
        - Camera support
        - HD Audio reset
- System and Power Management Signals
    - Reset out and Reset in
    - Power button in
    - Power source status
    - Module power state status
    - System management pins
    - Battery and battery charger management pins
    - Carrier Power On control
- Boot Source Select
    - Three pins to allow selection from Carrier Board
    - Select options to include boot from one of the following:
        - Module SPI
        - Module eMMC Flash
        - Module NAND / NOR Flash (vendor defined)
        - Module Remote Boot (Network or Serial Port, vendor defined)
        - Carrier SPI
        - Carrier SD Card
        - Carrier SATA
- JTAG functions for CPU debug and test are optionally implemented on separate small form factor connector(s)

3 MODULE INTERFACE REQUIRED AND OPTIONAL FEATURES

3.1 Required and Optional Feature Table

Required and optional features for an SMARC Module are summarized in the table below.

"*Shall*"	indicates a mandatory requirement
"***Should***"	indicates a recommended but not mandatory requirement
"***May***"	indicates a lesser used optional interface
"***Alternate***"	indicates an optional interface, implemented on pins shared with another use

Feature	Sub Feature	Requirement	Notes
LVDS LCD	18 bit single channel	***Should***	Default Display (serial LVDS)
	24 bit single channel – 18 bit compatible	***Should***	
	24 bit single channel – standard color map	***May***	
	24 bit dual channel – 18 bit compatible	***May***	
	24 bit dual channel – standard color map	***May***	
HDMI	HDMI display interface	***Should***	
DP on HDMI Pins		***May***	
DP++	DisplayPort++	***May***	
Camera	CSI0 – 2 lane	***Should***	
	CSI1 – 2 lane implementation	***May***	
	CSI1 – 4 lane implementation	***May***	
SDIO	SDIO (4 bit, for SD cards)	***Should***	***May*** be Carrier boot device
SPI	SPI0	***Should***	***May*** be Carrier boot device
	eSPI	***Should***	***May*** be Carrier boot device
Audio	I2S0	***Should***	
	HDA	***Should***	
I2C	Power Management	***Shall***	
	General Purpose	***Shall***	
	Camera	***Should***	
	LCD Display I/D	***Should***	

Serial Ports	SER0 (4 wire)	***Shall***	
	SER1 (2 wire)	***Shall***	
	SER2 (4 wire)	***Should***	
	SER3 (2 wire)	***Should***	
CAN Bus	CAN0	***May***	
	CAN1	***May***	
USB	USB0 - as USB 2.0 Client	***Should***	USB0 ***shall*** be implemented
	USB0 – as OTG	***May***	
	USB0 - as USB 2.0 Host	***May***	
	USB1 – as USB 2.0 Host	***Shall***	
	USB[2:5] - as USB 2.0 Host	***May***	
	USBss[2:3]	***May***	Fill order: first #2 then #3
	USB3 - as USB 3.0 Client / OTG	***May***	
PCIe	PCIE_A (x1 Gen 1 Root)	***Should***	
	PCIE_B (x1 Gen 1 Root)	***May***	
	PCIE_C (x1 Gen 1 Root)	***May***	
	PCIE_D (x1 Gen 1 Root)	***May***	
	PCIE_ Target operation	***May***	
	PCIE Gen 2 and Gen 3 operation	***May***	
SATA	SATA Gen 1	***Should***	***May*** be Carrier boot device
	SATA Gen 2 operation	***May***	
	SATA Gen 3 operation	***May***	
GBE	GBE0	***Should***	
	GBE1	***May***	
	IEEE 1588 Trigger Signals (GBE[0:1]_SDP)	***May***	
Watchdog	WDT Out	***Should***	
GPIO	GPIOs – 12x	***Shall***	
	GPIO interrupt capability – 12x	***Shall***	
	GPIO Camera Support	***Shall*** *(see Note)*	As appropriate for Module Camera implementation
	GPIO5 PWM capability	***Should***	
	GPIO6 Tachin capability	***Should***	
Management	System and power management features	***Shall***	See section 7.4.1 ‘x86 Power Management’ for details

Boot Select		***Shall***	
Force Recov		***Should***	See section 4.17 for details
JTAG	JTAG connector on Module	***May***	Some vendors prefer test point access
RTC		***Should***	

3.2 Feature Fill Order

Features ***shall*** be filled in a low – to – high order, based on the signal group names. For example, there are six possible USB ports, designated with signal prefixes USB0 to USB5. If a Module design implements only two USB, those would be USB0 and USB1. The PCIe links are designated PCIE_A, PCIE_B, PCIE_C and PCIE_D. If only one is implemented, it would be PCIE_A.

USB 3.0 port number 2 is the first in the fill order as the counting of USB 3.0 lines starts with number 2.

USB Super Speed operation is only defined for SMARC USB ports USB2 and USB3. Therefore USB2 is the first in the fill order for USB Super Speed (aka USB 3.0) implementations on SMARC.

4 SIGNAL DESCRIPTIONS

4.1 Signal Direction and Type Definitions

Direction	Type / Tolerance	Notes
Input		Input to the Module
Output		Output from the Module
Output OD		Open drain output from the Module
Bi-Dir		Bi-directional signal (can be input or output)
Bi-Dir OD		Bi-directional signal; output from the Module is open drain
	VDD_IN	Signal ***may*** be exposed to Module input voltage range (3.0 to 5.25V)
	CMOS 1.5V*	CMOS logic input and / or output, 1.5V I/O supply level or tolerance Used for HD Audio. ***Should*** be 1.8V signal tolerant.
	CMOS 1.8V	CMOS logic input and / or output, 1.8V I/O supply level or tolerance. Used for majority of SMARC I/O
	CMOS 3.3V	CMOS logic input and / or output, 3.3V I/O supply level or tolerance
	CMOS VDD_JTAG_IO	VDD_JTAG_IO is specific to the Module design. It ***may*** be 1.8V, 3.3V, or other value in the 0 to 3.3V range. The JTAG emulator adjusts to the VDD_JTAG_IO level provided by the Module, on the JTAG connector
	GBE MDI	Differential analog signaling for Gigabit Media Dependent Interface
	LVDS DP	LVDS signaling used for DisplayPort devices
	LVDS D-PHY	LVDS signaling used for MIPI CSI camera interfaces
	LVDS LCD	LVDS signaling used for LVDS LCD displays
	LVDS PCIE	LVDS signaling used for PCIE interfaces according to the PCI Express specification
	LVDS SATA	LVDS signaling used for SATA interfaces
	TMDS	LVDS signaling used for HDMI display interfaces
	USB	DC coupled differential signaling used for traditional (non- Super-Speed) USB signals
	USB SS	LVDS signaling used for Super Speed USB 3.0
	USB VBUS 5V	5V tolerant input for USB VBUS detection

4.2 Internal Display Interfaces

Single channel, dual channel or two single channel LVDS display panel interfaces are defined. The implementation of two single channel LVDS display interfaces is not expected to be common but is defined as an option for Module vendors. The LVDS interfaces support 18 and 24 bit display implementations. Alternatively, the SMARC LVDS pins may also be used to implement eDP or MIPI DSI display interfaces. See Sections 4.2.3 LVDS / eDP Pin Sharing and 4.2.4 LVDS / DSI Pin Sharing below. In a Module implementation with two single LVDS channels, the panel EDID proms would be in conflict and measures need to be taken to avoid this. One possible solution is that the 2nd LVDS EDID prom could be read over the I2C_GP pin pair rather than the I2C_LCD pin pair.

4.2.1 Primary LCD Display Support Signals

The signals in the table below support the LVDS LCD interfaces.

Signal Name	Direction	Type / Tolerance	Description
LCD[0:1]_VDD_EN	Output	CMOS 1.8V	High enables panel VDD
LCD[0:1]_BKLT_EN	Output	CMOS 1.8V	High enables panel backlight
LCD[0:1]_BKLT_PWM	Output	CMOS 1.8V	Display backlight PWM control
I2C_LCD_DAT	Bi-Dir OD	CMOS 1.8V	I2C data – to read LCD display EDID EEPROMs Be aware of possible EDID PROM address conflicts if multiple displays are implemented
I2C_LCD_CK	Output	CMOS 1.8V	I2C clock – to read LCD display EDID EEPROMs

4.2.2 Primary Display – 18 / 24 Bit LVDS LCD Dual Channel

The Module ***should*** implement an 18 / 24 bit dual channel LVDS output stream for the Primary display. This stream is usually created from the parallel RGB data, and usually carries the same display information, but in the serialized LVDS format. Control data (HS, VS, DE) are included in the LVDS stream.

Signal Name	Direction	Type / Tolerance	Description
LVDS[0:1]_[0:3]+ LVDS[0:1]_[0:3]-	Output	LVDS LCD	LVDS LCD data channel differential pairs
LVDS[0:1]_CK+ LVDS[0:1]_CK-	Output	LVDS LCD	LVDS LCD differential clock pair

All 18 bit TFT panels use the same LVDS color mapping. Only 3 data pairs (LVDS[0:1]_[0:2] +/-) and the clock pair are needed to drive an 18 bit TFT panel.

Unfortunately, there are two 24 bit LVDS color mappings in the industry:

- Most significant color bits on the 4th LVDS data pair (LVDS[0:1]_[3] +/- here). This is the more common 24 bit mapping. It is not compatible with the 18 bit LVDS color mapping.
- Least significant color bits on the 4th LVDS data pair. This is compatible with the 18 LVDS color mapping.

Modules that implement LVDS ***shall*** implement single channel 18 bit LVDS; ***should*** implement a 24 bit "18 bit compatible" LVDS mapping and ***may*** implement the "MS bit on 4th LVDS pair" mapping. The second LVDS channel ***may*** be implemented.

Details on LVDS color mappings are provided in ***Section 9 Appendix A: LVDS LCD Color*** Mappings***.***

4.2.3 LVDS / eDP Pin Sharing

Pins used for LVDS LCD support ***may*** alternatively be used to support up to two Embedded DisplayPorts. The AC coupling required for eDP operation ***shall*** be done off-Module.

LVDS Pin Pairs	LCD Support Pins / Other Pins	eDP Usage	Notes
LVDS0_0+ LVDS0_0-		eDP0_TX0+ eDP0_TX0-	eDP0 data pair 0
LVDS0_1+ LVDS0_1-		eDP0_TX1+ eDP0_TX1-	eDP0 data pair 1
LVDS0_2+ LVDS0_2-		eDP0_TX2+ eDP0_TX2-	eDP0 data pair 2
LVDS0_3+ LVDS0_3-		eDP0_TX3+ eDP0_TX3-	eDP0 data pair 3
LVDS0_CK+ LVDS0_CK-		eDP0_AUX+ eDP0_AUX-	eDP0 auxiliary channel pair
LVDS1_0+ LVDS1_0-		eDP1_TX0+ eDP1_TX0-	eDP1 data pair 0
LVDS1_1+ LVDS1_1-		eDP1_TX1+ eDP1_TX1-	eDP1 data pair 1
LVDS1_2+ LVDS1_2-		eDP1_TX2+ eDP1_TX2-	eDP1 data pair 2
LVDS1_3+ LVDS1_3-		eDP1_TX3+ eDP1_TX3-	eDP1 data pair 3
LVDS1_CK+ LVDS1_CK-		eDP1_AUX+ eDP1_AUX-	eDP1 auxiliary channel pair
	I2C_LCD_CK I2C_LCD_DAT		Optional - eDP panel information is usually obtained over the eDP AUX pair
	LCD[0:1]_VDD_EN	LCD[0:1]_VDD_EN	eDP 0/1 VDD_EN support over EDP_AUX channel is preferable
	LCD[0:1]_BKLT_EN	LCD[0:1]_BKLT_EN	eDP 0/1 BKLT_EN support over EDP_AUX channel is preferable
	LCD[0:1]_BKLT_PWM	LCD[0:1]_BKLT_PWM	eDP 0/1 BKLT_PWM support over EDP_AUX channel is preferable
		EDP[0:1]_HPD	eDP 0/1Hot Plug Detect pins

4.2.4 LVDS / DSI Pin Sharing

Pins used for LVDS LCD support ***may*** alternatively be used to support a MIPI DSI (Display Serial Interface). There is no AC coupling required for DSI operation.

LVDS Pin Pairs	LCD Support Pins / Other Pins	DSI Usage	Notes
LVDS0_0+ LVDS0_0-		DSI0_D0+ DSI0_D0-	DSI0 data pair 0
LVDS0_1+ LVDS0_1-		DSI0_D1+ DSI0_D1-	DSI0 data pair 1
LVDS0_2+ LVDS0_2-		DSI0_D2+ DSI0_D2-	DSI0 data pair 2
LVDS0_3+ LVDS0_3-		DSI0_D3+ DSI0_D3-	DSI0 data pair 3
LVDS0_CK+ LVDS0_CK-		DSI0_CLK+ DSI0_CLK-	DSI0 clock pair
LVDS1_0+ LVDS1_0-		DSI1_D0+ DSI1_D0-	DSI1 data pair 0
LVDS1_1+ LVDS1_1-		DSI1_D1+ DSI1_D1-	DSI1 data pair 1
LVDS1_2+ LVDS1_2-		DSI1_D2+ DSI1_D2-	DSI1 data pair 2
LVDS1_3+ LVDS1_3-		DSI1_D3+ DSI1_D3-	DSI1 data pair 3
LVDS1_CK+ LVDS1_CK-		DSI1_CLK+ DSI1_CLK-	DSI1 clock pair
	I2C_LCD_CK I2C_LCD_DAT		
	LCD[0:1]_VDD_EN	LCD[0:1]_VDD_EN	
	LCD[0:1]_BKLT_EN	LCD[0:1]_BKLT_EN	
	LCD[0:1]_BKLT_PWM	LCD[0:1]_BKLT_PWM	
	EDP[0:1]_HPD	DSI[0:1]_TE	DSI 0/1 tearing effect signal

4.2.5 Secondary (HDMI) Display

Signal Name	Direction	Type / Tolerance	Description
HDMI_D[0:2]+ HDMI_D[0:2]-	Output	TMDS	TMDS / HDMI data differential pairs
HDMI_CK+ HDMI_CK-	Output	TMDS	HDMI differential clock output pair
HDMI_HPD	Input	CMOS 1.8V	HDMI Hot Plug Detect input
HDMI_CTRL_DAT	Bi-Dir OD	CMOS 1.8V	I2C data line dedicated to HDMI
HDMI_CTRL_CK	Output OD	CMOS 1.8V	I2C clock line dedicated to HDMI

HDMI displays uses 5V I2C signaling. The Module HDMI_CTRL_DAT and HDMI_CTRL_CK signals need to be level translated on the Carrier from the Module 1.8V level. A similar consideration applies to the HDMI_HPD signal. There are a number of single chip devices on the market that perform ESD protection and control signal level shifting for HDMI interfaces. The Texas Instruments TPD12S016 is one such device.

4.2.6 DP++ Operation Over SMARC HDMI Pins

The SMARC HDMI pins ***may*** alternatively be used for DisplayPort++ (DP++) operation. This is Module vendor dependent.

DP++ Use	Direction	DP++ Description	Coupling / Tolerance	SMARC Signal Name for native HDMI
DP1_LANE0+ DP1_LANE0-	Output	DP Data Pair 0	AC Coupled ***off*** module	HDMI_D2+ HDMI_D2-
DP1_LANE1+ DP1_LANE1-	Output	DP Data Pair 1	AC Coupled ***off*** module	HDMI_D1+ HDMI_D1-
DP1_LANE2+ DP1_LANE2-	Output	DP Data Pair 2	AC Coupled ***off*** module	HDMI_D0+ HDMI_D0-
DP1_LANE3+ DP1_LANE3-	Output	DP Data Pair 3	AC Coupled ***off*** module	HDMI_CK+ HDMI_CK-
DP1_HPD	Input	DP Hot Plug Detect input	DC coupled CMOS 1.8V	HDMI_HPD
DP1_AUX-	Bi-Dir	DP AUX Channel (- part of pair)	AC Coupled ***on*** module	HDMI_CTRL_DAT
DP1_AUX+	Bi-Dir	DP AUX Channel (+ part of pair)	AC Coupled ***on*** module	HDMI_CTRL_CK
DP1_AUX_SEL	Input	Pulled to GND on Carrier for DP operation in Dual Mode (DP++) implementations. Driven to 1.8V on Carrier for HDMI operation. Terminated on Module through 1M resistor to GND.	DC coupled CMOS 1.8V	n/a

Dual Mode (HDMI and DisplayPort on the same pins) implementations ***may*** be realized. This is desirable for SOCs that natively implement this capability. With such SOCs, the primary Dual Mode implementation challenge is that the HDMI_CTRL_DAT and HDMI_CTRL_CK lines are DC coupled, but the DP_AUX+ /- pair must be AC coupled. A set of FET switches is usually used to sort this out. The FET gates can be controlled by the AUX_SEL pin function.

4.2.7 DP++

A DP++ interface can output signals that are formatted per either DP or HDMI / DVI protocols. The signal levels are DP compliant. For DP use, off-module coupling caps are needed on the 4 DP display data lanes. A Carrier Board level translator is usually needed for HDMI / DVI operation.

DP++ or DisplayPort++ (also named as Dual-mode DisplayPort) can directly output HDMI and DVI signals. The level adaptation can be implemented on the Carrier or via plug in cable adapter. In case of Carrier Board implementation a level shifter adjusts the I/O voltage to HDMI/DVI compliant signal levels. A dual-mode chipset switches to DVI/HDMI mode (4-lane main DisplayPort link and AUX channel) if a DVI or HDMI passive adapter is detected (by DP0_AUX_SEL).

Signal Name	Direction	Type / Tolerance	Description
DP0_LANE[0:3]+ DP0_LANE[0:3]-	Output	LVDS PCIE	Four DisplayPort differential pair lines
DP0_AUX+ DP0_AUX -	Bi-Dir	LVDS PCIE	Auxiliary channel used for link management and device control. Differential pair lines.
DP0_HPD	Input	CMOS 1.8V	Hot plug detection signal.
DP0_AUX_SEL	Input	CMOS 1.8V	Pulled to GND on Carrier for DP operation in Dual Mode implementations.

4.3 Camera Interfaces

SMARC 2.0 defines two MIPI CSI serial camera interfaces. The defined CSI0 interface supports up to two differential data lanes (CSI0_D[0:1]+/- signals). CSI1 ***may*** be implemented with up to four differential data lanes (CSI1_D[0:3]+/- signals) to support higher resolution cameras.

Both MIPI CSI interfaces support MIPI-CSI 2.0 but are also prepared to support the implementation of MIPI-CSI 3.0. Both standards continue to evolve (see **http://mipi.org/specifications/camera-interface**). While MIPI-CSI 2.0 utilizes an I2C bus (I2C_CAM[0:1]) to communicate with the camera the MIPI-CSI 3.0 uses a differential data lane (CSI[0:1]_TX+/-).

4.3.1 Camera Configurations

Configuration	CSI0	CSI1
Serial	CSI0 - 2 lanes MIPI CSI 2.0	CSI1 – 2 or 4 lanes MIPI-CSI 2.0
Alternative	CSI0 - 2 lanes MIPI CSI 3.0	CSI1 – 2 or 4 lanes MIPI-CSI 3.0

4.3.2 Camera Power Enables and Resets

Signal Name	Direction	Type / Tolerance	GPIO Use	Sanctioned Alternate Uses
GPIO0 / CAM0_PWR#	Bi-Dir	CMOS 1.8V	GPIO0	Camera 0 Power Enable, active low output.
GPIO1 / CAM1_PWR#	Bi-Dir	CMOS 1.8V	GPIO1	Camera 1 Power Enable, active low output
GPIO2 / CAM0_RST#	Bi-Dir	CMOS 1.8V	GPIO2	Camera 0 Reset, active low output
GPIO3 / CAM1_RST#	Bi-Dir	CMOS 1.8V	GPIO3	Camera 1 Reset, active low output

4.3.3 Camera I2C Support

The I2C_CAM_ port is intended to support serial cameras. Most contemporary cameras with I2C support allow a choice of two I2C address ranges.

Signal Name	Direction	Type / Tolerance	Description
I2C_CAM[0:1]_DAT	Bi-Dir OD	CMOS 1.8V	I2C data: Serial camera support link for serial cameras Alternative function: CSI[0:1]_TX- for MIPI CSI 3.0
I2C_CAM[0:1]_CK	Bi-Dir OD	CMOS 1.8V	I2C clock: Serial camera support link for serial cameras Alternative function: CSI[0:1]_TX+ for MIPI CSI 3.0

4.3.4 MIPI CSI Configuration CSI-2 and CSI-3

The newer version of the MIPI Camera Serial Interface CSI-3 no longer uses an I2C bus to transmit commands an configurations to the camera. A newly defined high speed differential signal pair is used instead.

Signal Name	Direction	Type / Tolerance	Description
CSI[0:1]_TX+ CSI[0:1]_TX-	Output	TMDS	Differential data pairs used for camera configurations

4.3.5 Serial Cameras In

Two MIPI CSI camera interfaces are supported. The CSI0 interface supports two lanes, the CSI1 interface supports 4 lanes. MIPI CSI 2.0 and MIPI CSI 3.0 are supported.

Signal Name	Direction	Type / Tolerance	Description
CSI0_D[0:1]+ CSI0_D[0:1]- CSI1_D[0:3]+ CSI1_D[0:3]-	Input	LVDS D-PHY	CSI differential data inputs
CSI[0:1]_CK+ CSI[0:1]_CK-	Input	LVDS D-PHY	CSI differential clock inputs
CAM_MCK	Output	CMOS 1.8V	Master clock output for CSI camera support (***may*** be used for CSI0 and / or CSI1)
I2C_CAM[0:1]_CK	Bi-Dir OD	CMOS 1.8V	Alternative use: MIPI-CSI 3.0 configuration CSI[0:1]_TX+
I2C_CAM[0:1]_DAT	Bi-Dir OD	CMOS 1.8V	Alternative use: MIPI-CSI 3.0 configuration CSI[0:1]_TX-

4.4 SDIO Card (4 bit) Interface

The Carrier SDIO Card ***may*** be selected as the Boot Device – see ***Section 4.17 Boot Select.***

Signal Name	Direction	Type / Tolerance	Description
SDIO_D[0:3]	Bi-Dir	CMOS 3.3V	4 bit data path
SDIO_CMD	Bi-Dir	CMOS 3.3V	Command line
SDIO_CK	Output	CMOS 3.3V	Clock
SDIO_WP	Input	CMOS 3.3V	Write Protect
SDIO_CD#	Input	CMOS 3.3V	Card Detect
SDIO_PWR_EN	Output	CMOS 3.3V	SD card power enable

Note: There are SD Cards with a 1.8V I/O voltage (UHS-I). SDIO controllers supporting these cards will adjust the I/O voltage levels.

4.5 SPI Interfaces

4.5.1 SPI0

The Carrier SPI0 device ***may*** be selected as the Boot Device – see ***Section 4.17 Boot Select.***

Signal Name	Direction	Type / Tolerance	Description
SPI0_CS0#	Output	CMOS 1.8V	SPI0 Master Chip Select 0 output Use to select Carrier SPI boot device
SPI0_CS1#	Output	CMOS 1.8V	SPI0 Master Chip Select 1 output
SPI0_CK	Output	CMOS 1.8V	SPI0 Master Clock output
SPI0_DIN	Input	CMOS 1.8V	SPI0 Master Data input (input to CPU, output from SPI device)
SPI0_DO	Output	CMOS 1.8V	SPI0 Master Data output (output from CPU, input to SPI device)

4.5.2 eSPI/SPI1

Signal Name	Direction	Type / Tolerance	Description
ESPI_CK	Output	CMOS 1.8V	ESPI Master Clock Output This pin provides the reference timing for all the serial input and output operations.
ESPI_CS[0:1]#	Output	CMOS 1.8V	ESPI Master Chip Select Outputs Driving Chip Select# low selects a particular eSPI slave for the transaction. Each of the eSPI slaves is connected to a dedicated Chip Select# pin.
ESPI_IO_[0:3]	Bi-Dir	CMOS 1.8V	ESPI Master Data Input / Outputs These are bi-directional input/output pins used to transfer data between master and slaves. In Single I/O mode, ESPI_IO_0 is the eSPI master output/eSPI slave input (MOSI) whereas ESPI_IO_1 is the eSPI master input/eSPI slave output (MISO).
ESPI_RESET#	Output	CMOS 1.8V	ESPI Reset Reset the eSPI interface for both master and slaves. eSPI Reset# is typically driven from eSPI master to eSPI slaves.
ESPI_ALERT[0:1]#	Input	CMOS 1.8V	This pin is used by eSPI slave to request service from eSPI master. Alert# is an open-drain output from the slave. This pin is optional for Single Master-Single Slave configuration where I/O[1] can be used to signal the Alert event.

4.6 Audio

Two audio interfaces are defined. One is pin shared with HDA, I2S1 from SMARC V1.1 has been deprecated.

The I2S interface is typically used for ARM processor implementation. HDA is typically used for x86 processor implementations. The HDA interface can also be used for a second I2S interface.

4.6.1 I2S

Two I2S interfaces are defined. These are typically used for digital audio I/O and other modest bandwidth functions. A common audio master clock signal is also defined.

Signal Name	Direction	Type / Tolerance	Description
I2S0_LRCK	Bi-Dir	CMOS 1.8V	Left& Right audio synchronization clock
I2S0_SDOUT	Output	CMOS 1.8V	Digital audio Output
I2S0_SDIN	Input	CMOS 1.8V	Digital audio Input
I2S0_CK	Bi-Dir	CMOS 1.8V	Digital audio clock
AUDIO_MCK	Output	CMOS 1.8V	Master clock output to Audio codecs

4.6.2 HDA / I2S

Signal Name	Direction	Type / Tolerance	Description
HDA_SYNC	Bi-Dir	**CMOS 1.5V / 1.8V***	Left& Right audio synchronization clock / HDA sync Alternative use: I2S2_LRCK
HDA_SDO	Output	**CMOS 1.5V / 1.8V***	I2S Digital audio Output / High Definition Audio data out Alternative use: I2S2_SDOUT
HDA_SDI	Input	**CMOS 1.5V / 1.8V***	I2S Digital audio Input / High Definition Audio data in Alternative use: I2S2_SDI
HDA_CK	Bi-Dir	**CMOS 1.5V / 1.8V***	I2S Digital audio clock/ High Definition Audio clock Alternative use: I2S2_CK
HDA_RST#	Output	**CMOS 1.5V / 1.8V***	HDA reset output (by means of GPIO4)

Note: The numbering of the secondary, alternative I2S interface is #2 because the I2S interface #1 from SMARC 1.1 was removed for SMARC 2.0.

Per the HD Audio specification, HD Audio ***may*** be run at either 1.5V or 3.3V. SMARC requires 1.5V or 1.8V HD Audio signaling. Please check with your module vendor if 1.5V or 1.8V are supported and use an audio codec that is capable to support the regarding I/O voltage. The SMARC HD Audio pins are shared with the I2S2 pins, which are defined to be 1.8V. This specification ignores the discrepancy between the 1.5V and 1.8V signaling, as the chance of damage in mismatched systems is negligible.

ARM SOCs generally run I2S audio and will likely use 1.8V signaling. X86 SOCs generally run 1.5V signal levels on the HD Audio interface.

4.7 I2C Interfaces

The Module supports six I2C interfaces, per the following table. Except for the LCD and HDMI Module I2C interfaces, the I2C ports ***should*** be multi-master capable. Data rates of 100 kHz and 400 kHz ***should*** be supported.

I2C Port	Primary Purpose	Alternate Use	I/O Voltage Level
I2C_PM	Power Management support	System configuration management	CMOS 1.8V
I2C_CAM0 I2C_CAM1	Camera support	General Purpose	CMOS 1.8V
I2C_GP	General purpose use		CMOS 1.8V
I2C_LCD	LCD display support	General Purpose	CMOS 1.8V
HDMI_CTRL	HDMI control		CMOS 1.8V

All I2C interfaces but the I2C_GP interface are described in the section served by that I2C link (LCD, HDMI, Camera Interface, etc). The I2C_GP Module interface consists of the following two pins:

Signal Name	Direction	Type / Tolerance	Description
I2C_GP_CK	Bi-Dir OD	CMOS 1.8V	I2C General Purpose clock signal
I2C_GP_DAT	Bi-Dir OD	CMOS 1.8V	I2C General Purpose data signal

4.8 Asynchronous Serial Ports

Module pins for up to four asynchronous serial ports are defined. The ports are designated SER0 – SER3. Ports SER0 and SER2 are 4 wire ports (2 data lines and 2 handshake lines). Ports SER1 and SER3 are 2 wire ports (data only).

Signal Name	Direction	Type / Tolerance	Description
SER[0:3]_TX	Output	CMOS 1.8V	Asynchronous serial port data out
SER[0:3]_RX	Input	CMOS 1.8V	Asynchronous serial port data in
SER[0]_RTS#	Output	CMOS 1.8V	Request to Send handshake line for SER0
SER[0]_CTS#	Input	CMOS 1.8V	Clear to Send handshake line for SER0
SER[2]_RTS#	Output	CMOS 1.8V	Request to Send handshake line for SER2
SER[2]_CTS#	Input	CMOS 1.8V	Clear to Send handshake line for SER2

4.9 CAN Bus

Signal Name	Direction	Type / Tolerance	Description
CAN[0:1]_TX	Output	CMOS 1.8V	CAN Transmit output
CAN[0:1]_RX	Input	CMOS 1.8V	CAN Receive input

4.10 USB Interfaces

SMARC 2.0 provides six sets of USB 2.0 signals and two sets of USB 3.0 Super Speed signals.

USB OTG and USB Client functionalities are also supported.

USB 3.0 is supported for the USB ports 2 and 3. For implementation of USB 3.0 OTG or USB 3.0 host USB3 ***may*** be used.

The USB0 port ***shall*** be available as a USB 2.0 client. It ***may*** also be available as an OTG port (and, by extension, as a host), or as a host (some SOCs allow a USB port to be configured as client or host, but do not support full OTG functionality).

4.10.1 USB Signal Assignments

	USB 2.0	USB 3.0	OTG/VBUS	Client Capability
USB0	x		x	x
USB1	x			
USB2	x	x		
USB3	x	x	x	x
USB4	x			
USB5	x			

4.10.2 USB Signals

Signal Name	Direction	Type / Tolerance	Description
USB[0:5]+ USB[0:5]-	Bi-Dir	USB	Differential USB 2.0 data pairs
USB[0:5]_EN_OC#	Bi-Dir OD	CMOS 3.3V	Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation. A pull-up ***shall*** be present on the Module to a 3.3V rail. The pull-up rail ***may*** be switched off to conserve power if the USB port is not in use. Further details ***may*** be found in Section ***4.10.3 USB[0:5]_EN***_OC# Discussion below.
USB0_VBUS_DET USB3_VBUS_DET	Input	USB VBUS 5V	USB host power detection, when this port is used as a device.
USB0_OTG_ID USB3_OTG_ID	Input	CMOS 3.3V	USB OTG ID input, active high.
USB[2:3]SSRX- USB[2:3]SSRX+	Input	USB SS	Receive signal differential pairs for SuperSpeed USB data Coupling caps for RX pairs are ***off***-Module
USB[2:3]SSTX- USB[2:3]SSTX+	Output	USB SS	Transmit signal differential pairs for SuperSpeed USB data Coupling caps for RX pairs are ***off***-Module

4.10.3 USB[0:5]_EN_OC# Discussion

The Module USB[0:5]_EN_OC# pins are multi-function Module pins, with a pull-up to a 3.3V rail on the Module, an OD driver on the Module, and, if the OC# (over-current) monitoring function is implemented on the Carrier, an OD driver on the Carrier. The use is as follows:

1) On the Carrier board, for external plug-in USB peripherals (USB memory sticks, cameras, keyboards, mice, etc.) USB power distribution is typically handled by USB power switches such as the Texas Instruments TPS2052B or the Micrel MIC2026-1 or similar devices. The Carrier implementation is more straightforward if the Carrier USB power switches have active–high power enables and active low open drain OC# outputs (as the TI and Micrel devices referenced do). The USB power switch Enable and OC# pins for a given USB channel are tied together on the Carrier. The USB power switch enable pin must function with a low input current. The TI and Micrel devices referenced above require 1 microampere or less, at a 3.3V enable voltage level.
2) The Module drives USB[0:5]_EN_OC# low to disable the power delivery to the USB[0:5] device.
3) The Module floats USB[0:5]_EN_OC# to enable power delivery. The line is pulled to 3.3V by the Module pull-up, enabling the Carrier board USB power switch. If there is a USB over-current condition, the Carrier board USB power switch drives the USB[0:5]_EN_OC# line low. This removes the over-current condition (by disabling the USB switch enable input), and allows Module software to detect the over-current condition. The Module software ***should*** look for a falling edge interrupt on USB[0:5]_EN_OC#, while the port is enabled, to detect the OC# condition. The OC# condition will not last long, as the USB power switch is disabled when the switch IC detects the OC# condition. If the USB power to the port is disabled (USB[0:5]_EN_OC# is driven low by the Module) then the Module software must be aware that the port is disabled, and the low input value on the port does not indicate an over-current condition (because the port power is disabled).If the USB power to the port is disabled, then the Module ***may*** remove the 3.3V pull-up voltage to the USB[0:5]_EN_OC# node, to save the current drain through the pull-up resistor. This is optional and Module design dependent.

Carrier Board USB peripherals that are not removable often do ***not*** make use of USB power switches with current limiting and over-current detection. It is usually deemed un-necessary for non-removable devices. In these cases, the USB[0:5]_EN_OC# pins ***may*** be left unused, or they ***may*** be used as USB[0:5] power enables, without making use of the over-current detect Module input feature.

4.11 PCI Express

The Module ***may*** implement up to four PCIe lanes. The links ***may*** be PCIe Gen 1, 2 or 3, as the Module chip or chipset allows.

The Module PCIe links are primarily PCIe Root Complexes. If the chipset allows it, the PCIe link(s) ***may*** alternatively be configured as a PCIe target(s). This is Module vendor specific.

Modules ***should*** implement the PCIe Link A port. Modules ***may*** implement the PCIe Links B, C and D ports. Fill order is A, B, C then D.

Signal Name	Direction	Type / Tolerance	Description
PCIE_[A:D]_TX+ PCIE_[A:D]_TX-	Output	LVDS PCIe	Differential PCIe Link transmit data pair Series coupling caps ***shall*** be on the Module Caps ***should*** be 0402 package 0.1uF
PCIE_[A:D]_RX+ PCIE_[A:D]_RX-	Input	LVDS PCIe	Differential PCIe Link receive data pair 0 No coupling caps on Module
PCIE_[A:C]_REFCK+ PCIE_[A:C]_REFCK-	Output	LVDS PCIe	Differential PCIe Link reference clock output DC coupled
PCIE_[A:C]_RST#	Output	CMOS 3.3V	PCIe Port reset output
PCIE_WAKE#	Input	CMOS 3.3V	PCIe wake up interrupt to host – common to PCIe links A, B, C, D – pulled up or terminated on Module

4.11.1 PCI Express Link Width

A connection between any two PCIe devices is known as a link, and is built up from a collection of one or more lanes. All devices ***shall*** support at least one single lane (x1) link. Devices may optionally support wider links composed of 2 or 4 lanes. Therefore the root complex ***may*** support different link width additionally to the x1 configuration.

SMARC PCIe Lane	Possible Link Configuration			
PCIe A	x1	x1	x2	x4
PCIe B	x1	x1		
PCIe C	x1	x2	x2	
PCIe D	x1			

SMARC PCIe Lane	REFCK and RST Assignments			
PCIe A	PCIE_A_REFCK PCIE_A_RST#	PCIE_A_REFCK PCIE_A_RST#	PCIE_A_REFCK PCIE_A_RST#	PCIE_A_REFCK PCIE_A_RST#
PCIe B	PCIE_B_REFCK PCIE_B_RST#	PCIE_B_REFCK PCIE_B_RST#		
PCIe C	PCIE_C_REFCK PCIE_C_RST#	PCIE_C_REFCK PCIE_C_RST#	PCIE_B_REFCK PCIE_B_RST#	
PCIe D	to be generated via buffer from PCIe A signals			

4.12 SATA

The Module definition allows for one SATA port. The port ***may*** be SATA Gen 1, 2 or 3 as the Module chip or chipset allows.

The Carrier SATA device ***may*** be selected as the Boot Device – see ***Section 4.17***

Signal Name	Direction	Type / Tolerance	Description
SATA_TX+ SATA_TX-	Output	SATA	Differential SATA 0 transmit data Pair 0402 series coupling caps ***shall*** be on Module
SATA_RX+ SATA_RX-	Input	SATA	Differential SATA 0 transmit data 0402 series coupling caps ***shall*** be on Module
SATA_ACT#	Output OD	CMOS 3.3V Tolerance	Active low SATA activity indicator If implemented, ***shall*** be able to sink 24mA or more Carrier LED current

4.13 Ethernet

The SMARC 2.0 pin-out supports two gigabit Ethernet capable ports. If only one is implemented, it ***should*** be GBE0.

Signal Name	Direction	Type / Tolerance	Description
GBE[0:1]_MDI0+ GBE[0:1]_MDI0-	Bi-Dir	GBE MDI	Bi-directional transmit/receive pair 0 to magnetics (Media Dependent Interface)
GBE[0:1]_MDI1+ GBE[0:1]_MDI1-	Bi-Dir	GBE MDI	Bi-directional transmit/receive pair 1 to magnetics (Media Dependent Interface)
GBE[0:1]_MDI2+ GBE[0:1]_MDI2-	Bi-Dir	GBE MDI	Bi-directional transmit/receive pair 2 to magnetics (Media Dependent Interface)
GBE[0:1]_MDI3+ GBE[0:1]_MDI3-	Bi-Dir	GBE MDI	Bi-directional transmit/receive pair 3 to magnetics (Media Dependent Interface)
GBE[0:1]_LINK100#	Output OD	CMOS 3.3V Tolerance	Link Speed Indication LED for 100Mbps ***Shall*** be able to sink 24mA or more Carrier LED current
GBE[0:1]_LINK1000#	Output OD	CMOS 3.3V Tolerance	Link Speed Indication LED for 1000Mbps ***Shall*** be able to sink 24mA or more Carrier LED current
GBE[0:1]_LINK_ACT#	Output OD	CMOS 3.3V Tolerance	Link / Activity Indication LED Driven low on Link (10, 100 or 1000 mbps) Blinks on Activity ***Shall*** be able to sink 24mA or more Carrier LED current
GBE[0:1]_CTREF	Output	Reference Voltage	Center-Tap reference voltage for Carrier board Ethernet magnetic (if required by the Module GBE PHY)
GBE[0:1]_SDP	Bi-Dir	CMOS 3.3V Tolerance	IEEE 1588 Trigger Signal. For hardware implementation of PTP (precision time protocol). This is typically implemented by the software-defined pins from the Ethernet controller. The SDP pins can be used for IEEE1588 auxiliary device connections and for other miscellaneous hardware or software-control purposes.

4.14 Watchdog

Signal Name	Direction	Type / Tolerance	Description
WDT_TIME_OUT#	Output	CMOS 1.8V	Watch-Dog-Timer Output

4.15 GPIO

Twelve Module pins are allocated for GPIO (general purpose input / output) use. All pins ***should*** be capable of bi-directional operation. A preferred direction of operation is assigned, with half of them (GPIO0 – GPIO5) recommended for use as outputs and the remainder (GPIO6 – GPIO11) as inputs.

At Module power-up, the state of the GPIO pins ***may not*** be defined, and ***may*** briefly be configured in the "wrong" state, before boot loader code corrects them. Carrier designers ***should*** be aware of this and plan accordingly. Module designers ***should*** generally choose pins that are tri-stated or are inputs during power up and reset, but this ***may not*** always be the case.

All GPIO pins ***should*** be weakly pulled up to 1.8V. If the pull-ups are implemented as discrete resistors, or resistor packs, a value of 470K ***should*** be used. SOC internal pull-up / current source features ***may*** be used instead of external resistors.

All GPIO pins ***shall*** be capable of generating interrupts. The interrupt characteristics (edge or level sensitivity, polarity) are generally configurable in the SOC register set.

Signal Name	Direction	Preferred Direction	Type / Tolerance	GPIO Use	Sanctioned Alternate Uses
GPIO0 / CAM0_PWR#	Bi-Dir	Output	CMOS 1.8V	GPIO0	Camera 0 Power Enable, active low output
GPIO1 / CAM1_PWR#	Bi-Dir	Output	CMOS 1.8V	GPIO1	Camera 1 Power Enable, active low output
GPIO2 / CAM0_RST#	Bi-Dir	Output	CMOS 1.8V	GPIO2	Camera 0 Reset, active low output
GPIO3 / CAM1_RST#	Bi-Dir	Output	CMOS 1.8V	GPIO3	Camera 1 Reset, active low output
GPIO4 / HDA_RST#	Bi-Dir	Output	CMOS 1.8V	GPIO4	HD Audio Reset, active low output
GPIO5 / PWM_OUT	Bi-Dir	Output	CMOS 1.8V	GPIO5	PWM output
GPIO6 / TACHIN	Bi-Dir	Input	CMOS 1.8V	GPIO6	Tachometer input (used with the GPIO5 PWM)
GPIO7	Bi-Dir	Input	CMOS 1.8V	GPIO7	
GPIO8	Bi-Dir	Input	CMOS 1.8V	GPIO8	
GPIO9	Bi-Dir	Input	CMOS 1.8V	GPIO9	
GPIO10	Bi-Dir	Input	CMOS 1.8V	GPIO10	
GPIO11	Bi-Dir	Input	CMOS 1.8V	GPIO11	

4.16 Management Pins

The input pins listed in this table are all active low and are meant to be driven by OD (open drain) devices on the Carrier. The Carrier either floats the line or drives it to GND. No Carrier pull-ups are needed. The pull-up functions are performed on the Module. The voltage rail that these lines are pulled to on the Module varies, depending on the design, and ***may*** be anywhere from 1.8V to 5.25V.

Switches to GND ***may*** be used instead of OD drivers for lines such as PWR_BTN# and RESET_IN#.

Signal Name	Direction	Type / Tolerance	Description
VIN_PWR_BAD#	Input	CMOS VDD_IN	Power bad indication from Carrier board. Module and Carrier power supplies (other than Module and Carrier power supervisory circuits) ***shall not*** be enabled while this signal is held low by the Carrier. Pulled up on Module. Driven by OD part on Carrier.
CARRIER_PWR_ON	Output	CMOS 1.8V	Carrier board circuits (apart from power management and power path circuits) ***should not*** be powered up until the Module asserts the CARRIER_PWR_ON signal. On x86 designs this pin ***should*** utilize the SUS_S5# signal, but then it ***shall*** maintain still the CARRIER_PWR_ON functionality to avoid back driving.
CARRIER_STBY#	Output	CMOS 1.8V	The Module ***shall*** drive this signal low when the system is in a standby power state. On x86 designs this pin ***should*** utilize the SUS_S3# signal.
RESET_OUT#	Output	CMOS 1.8V	General purpose reset output to Carrier board.
RESET_IN#	Input	CMOS 1.8V	Reset input from Carrier board. Carrier drives low to force a Module reset, floats the line otherwise. Pulled up on Module. Driven by OD part on Carrier.
POWER_BTN#	Input	CMOS 1.8V	Power-button input from Carrier board. Carrier to float the line in in-active state. Active low, level sensitive. ***Should*** be de-bounced on the Module Pulled up on Module. Driven by OD part on Carrier.
SLEEP#	Input	CMOS 1.8V	Sleep indicator from Carrier board. ***May*** be sourced from user Sleep button or Carrier logic. Carrier to float the line in in-active state. Active low, level sensitive. ***Should*** be de-bounced on the Module. Pulled up on Module. Driven by OD part on Carrier.
LID#	Input	CMOS 1.8V	Lid open/close indication to Module. Low indicates lid closure (which system ***may*** use to initiate a sleep state). Carrier to float the line in in-active state. Active low, level sensitive. ***Should*** be de-bounced on the Module Pulled up on Module. Driven by OD part on Carrier.
BATLOW#	Input	CMOS 1.8V	Battery low indication to Module. Carrier to float the line in in-active state. Pulled up on Module. Driven by OD part on Carrier.
I2C_PM_DAT I2C_PM_CK	Bi-Dir OD	CMOS 1.8V	Power management I2C bus data and clock. On x86 systems these serve as SMB data and clock.
CHARGING#	Input	CMOS 1.8V	Held low by Carrier during battery charging. Carrier to float the line when charge is complete. Pulled up on Module. Driven by OD part on Carrier.
CHARGER_PRSNT#	Input	CMOS 1.8V	Held low by Carrier if DC input for battery charger is present. Pulled up on Module. Driven by OD part on Carrier.
TEST#	Input	CMOS 1.8V	Held low by Carrier to invoke Module vendor specific test function(s). Pulled up on Module. Driven by OD part on Carrier.
SMB_ALERT_1V8#	Input	CMOS 1.8V	SM Bus Alert# (interrupt) signal

4.17 Boot Select

Three Module pins allow the Carrier board user to select from eight possible boot devices. Three are Module devices, and four are Carrier devices, and one is a remote device. The pins ***shall*** be weakly pulled up on the Module and the pin states decoded by Module logic. The Carrier ***shall*** either leave the Module pin Not Connected ("Float" in the table below) or ***shall*** pull the pin to GND, per the second table below.

A "Force Recovery" provision exists, per the pin description below.

Signal Name	Direction	Type / Tolerance	Description
BOOT_SEL[0:2]#	Input	CMOS 1.8V	Input straps determine the Module boot device. Pulled up on Module. Driven by OD part on Carrier.
FORCE_RECOV#	Input	CMOS 1.8V	Low on this pin allows non-protected segments of Module boot device to be rewritten / restored from an external USB Host on Module USB0. The Module USB0 operates in Client Mode when in the Force Recovery function is invoked. Pulled high on the Module. For SOCs that do not implement a USB based Force Recovery functions, then a low on the Module FORCE_RECOV# pin ***may*** invoke the SOC native Force Recovery mode – such as over a Serial Port. For x86 systems this signal ***may*** be used to load BIOS defaults. Pulled up on Module. Driven by OD part on Carrier.

	Carrier Connection			Boot Source
	BOOT_SEL2#	BOOT_SEL1#	BOOT_SEL0#	
0	GND	GND	GND	Carrier SATA
1	GND	GND	Float	Carrier SD Card
2	GND	Float	GND	Carrier eSPI (CS0#)
3	GND	Float	Float	Carrier SPI (CS0#)
4	Float	GND	GND	Module device (NAND, NOR) – vendor specific
5	Float	GND	Float	Remote boot (GBE, serial) – vendor specific
6	Float	Float	GND	Module eMMC Flash
7	Float	Float	Float	Module SPI

Note: The boot sources shown above are Module options, and ***may not*** be available on all Module designs.

The definition of "boot" is left to the Module designer. Some designs ***may*** literally implement some or all of the table above, such that the first off-SOC code fetches come from the devices listed above. Alternatively, some designs ***may*** always fetch the first few off-SOC instructions from a fixed device, likely a SPI Flash EEPROM, and then re-direct the execution to another device per the table above.

4.18 IO Levels

4.18.1 Default I/O 1.8V

In the interest of minimizing system power, the majority of SMARC I/O is at a 1.8V level. Most SOCs used for SMARC systems are optimized for 1.8V I/O. Recall that the power required to charge and discharge the pin capacitance of a target IC is proportional to the **square** of the I/O voltage.

4.18.2 Signals at 3.3V

A few SMARC interfaces run at 3.3V to interface with industry standard devices on the Carrier that run at 3.3V. Such interfaces include the SD Card signals (SDIO_ prefix); the USB[0:5]_EN_OC# signals; the USB[0,3]_OTG_ID signals; the PCIE support signals (x = A, B, C; support includes PCIE_[A:C]_CKREQ# and PCIE_[A:C]_RST#); the PCIE_WAKE# signal; the SATA_ACT# signal and the GBE[0:1]_LINK_100#, GBE[0:1]_LINK_1000#, GBE[0:1]_LINK_ACT# signals.

4.18.3 Signals at 5V

The USB[0,3]_VBUS_DET signals are 5V tolerant.

4.19 Power and GND

Signal Name	Type / Tolerance	Use
VDD_IN	Power In	Module power input voltage - 3.0V min to 5.25V max
GND	Ground	Module signal and power return, and GND reference
VDD_RTC	Power In Power Out (when charging a Super Cap)	Low current RTC circuit backup power – 3.0V nominal ***May*** be sourced from a Carrier based Lithium cell or Super Cap. See ***Section 7.3 RTC Voltage Rail*** for an important safety note on the implementation of lithium backup batteries.

4.20 JTAG

A CPU JTAG interface ***may*** be implemented on the Module, using a small form factor R/A SMT connector. The JTAG pins are used to allow test equipment and circuit emulators to have access to the Module CPU. The pin-out shown below ***may*** be used:

JTAG Conn Pin Number	Signal Name	Direction	Type / Tolerance	Description
1	VDD_JTAG_IO	Power	Power	JTAG I/O Voltage (sourced by Module)
2	JTAG_TRST#	Input	CMOS VDD_JTAG_IO	JTAG Reset, active low
3	JTAG_TMS	Input	CMOS VDD_JTAG_IO	JTAG mode select
4	JTAG_TDO	Output	CMOS VDD_JTAG_IO	JTAG data out
5	JTAG_TDI	Input	CMOS VDD_JTAG_IO	JTAG data in
6	JTAG_TCK	Input	CMOS VDD_JTAG_IO	JTAG clock
7	JTAG_RTCK	Input	CMOS VDD_JTAG_IO	JTAG return clock
8	GND			
9	MFG_MODE#	Input	CMOS VDD_JTAG_IO	Pulled low to allow in-circuit SPI ROM update
10	GND			

The Module JTAG connector ***may*** be implemented with a JST SH series 1mm pitch R/A wire mount header (JST SM10B-SRSS-TB).

4.21 Module Terminations

4.21.1 Module Input Terminations - General

Except as noted in the tables in the following two sub-sections, all Module inputs ***shall*** be terminated such that if the interface is used or not used, the proper pull up or pull down resistor or other termination mechanism is on the Module, either as a component on the PCB or as part of an IC used on the Module. If the Carrier Board does not use a particular interface, it ***shall*** be possible to leave the Module pin Not Connected on the Carrier. ***Except*** as noted below, pull-up resistors on the Carrier board for Module inputs are generally not required and ***should*** be avoided. They can cause Carrier to Module leakage problems.

4.21.2 Module Terminations – Specific Recommendations

The Module signals listed below ***shall*** be terminated on the Module. The terminations ***should*** follow the guidance given in the table below, although the final decision on specific component values and types is left to the Module designer.

Signal Name	Series Termination (On Module)	Parallel Termination (On Module)	Notes
GPIO[0:11]		470K pull-ups to 1.8V	SOC internal pull-ups ***may*** be used.
HDMI_CTRL_DAT		100K pull-up to 1.8V	Carrier pull-up required
HDMI_CTRL_CK		100K pull-up to 1.8V	Carrier pull-up required
I2C_CAM[0:1]_DAT		2.2K pull-up to 1.8V	
I2C_CAM[0:1]_CK		2.2K pull-up to 1.8V	
I2C_GP_DAT		2.2K pull-up to 1.8V	
I2C_GP_CK		2.2K pull-up to 1.8V	
I2C_LCD_DAT		2.2K pull-up to 1.8V	
I2C_LCD_CK		2.2K pull-up to 1.8V	
I2C_PM_DAT		2.2K pull-up to 1.8V	
I2C_PM_CK		2.2K pull-up to 1.8V	
PCIE_[A:D]_TX+	0.2 uF capacitor		
PCIE_[A:D]_TX-	0.2 uF capacitor		
SATA0_TX+	10 nF capacitor		
SATA0_TX-	10 nF capacitor		
SATA0_RX+	10 nF capacitor		
SATA0_RX-	10 nF capacitor		
SDIO_CD#		10K pull-up to 3.3V	
SDIO_WP		10K pull-up to 3.3V	
USB[0:5]_EN_OC#		10K pull-up to 3.3V or a switched 3.3V rail on the Module	Switched 3.3V: if a USB channel is not used, then the USB[0:5]_EN_OC# pull-up rail ***may*** be held at GND to prevent leakage currents.
All Other Inputs			All other inputs ***should*** be weakly terminated to their inactive states.

4.22 Carrier / Off-Module Terminations

The following Carrier terminations are required, if the relevant interface is used. If unused, the SMARC Module pins ***may*** be left un-connected.

Module Signal Group Name	Carrier Series Termination	Carrier Parallel Termination	Notes
GBE[0:1]_MDI[0:3][+:-]	Magnetics module appropriate for 10/100/1000 GBE transceivers	Secondary side center tap terminations appropriate for Gigabit Ethernet implementations	
GBE[0:1]_LINK (GBE status LED sinks)		If used, current limiting resistors and diodes to pulled to a positive supply rail	The open drain GBE status signals, GBE[0:1]_LINK100#, GBE[0:1]_LINK1000# and GBE[0:1]_LINK_ACT#, if used, need Carrier based current limiting resistors and LEDs. The LED ***may*** be integrated into a Carrier RJ45 jack. A resistor of 68 ohms, and a LED with the anode tied to Carrier 3.3V, is typical.
HDMI_CTRL_DAT HDMI_CTRL_CK		Pull-ups to 1.8V on each of these lines is required on the Carrier. The pull-ups ***may*** be part of an integrated HDMI ESD protection and control-line level shift device, such as the Texas Instruments TPD12S016. If discrete Carrier pull-ups are used, they ***should*** be 10K.	
DP[0:1]_AUX_SEL		Carrier DP[0:1]_AUX_SEL should be connected to pin 13 of the DisplayPort connector to enable a dual-mode DisplayPort interface.	
DP[0:1]_LANE[0:3]+ DP[0:1]_LANE[0:3]-		DC blocking capacitors shall be placed on the Carrier for the DP[0:1]_LANE[0:3] signals.	
DP[0:1]_HPD		The carrier ***shall*** include a blocking FET on DP[0:1]_HPD to prevent back-drive current from damaging the module.	
eDP[0:1]_TX[0:3]+ eDP[0:1]_TX[0:3]-		DC blocking capacitors ***shall*** be placed on the Carrier for the eDP[0:1]_TX[0:3] signals.	
DSI[0:1]_D[0:3]+ DSI[0:1]_D[0:3]+		No blocking capacitors or termination required. Layout for 90 Ohms differential impedance.	
LVDS LCD		100 ohm resistive termination across the differential pairs at the endpoint of the signal path, usually on the display assembly	
PCIE_[A:D]_RX+ PCIE_[A:D]_RX-	Series coupling caps near the TX pins of the Carrier board PCIe device (0.2µF)		

5 MODULE PIN-OUT MAP

5.1 Module Pin-Out

P-PIN	Primary (Top) Side	S-Pin	Secondary (Bottom) Side
		S1	CSI1_TX+ / I2C_CAM1_CK
P1	SMB_ALERT_1V8#	S2	CSI1_TX- / I2C_CAM1_DAT
P2	GND	S3	GND
P3	CSI1_CK+	S4	RSVD
P4	CSI1_CK-	S5	CSI0_TX- / I2C_CAM0_CK
P5	GBE1_SDP	S6	CAM_MCK
P6	GBE0_SDP	S7	CSI0_TX+ / I2C_CAM0_DAT
P7	CSI1_RX0+	S8	CSI0_CK+
P8	CSI1_RX0-	S9	CSI0_CK-
P9	GND	S10	GND
P10	CSI1_RX1+	S11	CSI0_RX0+
P11	CSI1_RX1-	S12	CSI0_RX0-
P12	GND	S13	GND
P13	CSI1_RX2+	S14	CSI0_RX1+
P14	CSI1_RX2-	S15	CSI0_RX1-
P15	GND	S16	GND
P16	CSI1_RX3+	S17	GBE1_MDI0+
P17	CSI1_RX3-	S18	GBE1_MDI0-
P18	GND	S19	GBE1_LINK100#
P19	GBE0_MDI3-	S20	GBE1_MDI1+
P20	GBE0_MDI3+	S21	GBE1_MDI1-
P21	GBE0_LINK100#	S22	GBE1_LINK1000#
P22	GBE0_LINK1000#	S23	GBE1_MDI2+
P23	GBE0_MDI2-	S24	GBE1_MDI2-
P24	GBE0_MDI2+	S25	GND
P25	GBE0_LINK_ACT#	S26	GBE1_MDI3+
P26	GBE0_MDI1-	S27	GBE1_MDI3-
P27	GBE0_MDI1+	S28	GBE1_CTREF
P28	GBE0_CTREF	S29	PCIE_D_TX+
P29	GBE0_MDI0-	S30	PCIE_D_TX-
P30	GBE0_MDI0+	S31	GBE1_LINK_ACT#
P31	SPI0_CS1#	S32	PCIE_D_RX+
P32	GND	S33	PCIE_D_RX-
P33	SDIO_WP	S34	GND
P34	SDIO_CMD	S35	USB4+

P-PIN	Primary (Top) Side
P35	SDIO_CD#
P36	SDIO_CK
P37	SDIO_PWR_EN
P38	GND
P39	SDIO_D0
P40	SDIO_D1
P41	SDIO_D2
P42	SDIO_D3
P43	SPI0_CS0#
P44	SPI0_CK
P45	SPI0_DIN
P46	SPI0_DO
P47	GND
P48	SATA_TX+
P49	SATA_TX-
P50	GND
P51	SATA_RX+
P52	SATA_RX-
P53	GND
P54	ESPI_CS0#
P55	ESPI_CS1#
P56	ESPI_CK
P57	ESPI_IO_0
P58	ESPI_IO_1
P59	GND
P60	USB0+
P61	USB0-
P62	USB0_EN_OC#
P63	USB0_VBUS_DET
P64	USB0_OTG_ID
P65	USB1+
P66	USB1-
P67	USB1_EN_OC#
P68	GND
P69	USB2+
P70	USB2-
P71	USB2_EN_OC#
P72	RSVD
P73	RSVD

S-Pin	Secondary (Bottom) Side
S36	USB4-
S37	USB3_VBUS_DET
S38	AUDIO_MCK
S39	I2S0_LRCK
S40	I2S0_SDOUT
S41	I2S0_SDIN
S42	I2S0_CK
S43	ESPI_ALERT0#
S44	ESPI_ALERT1#
S45	RSVD
S46	RSVD
S47	GND
S48	I2C_GP_CK
S49	I2C_GP_DAT
S50	HDA_SYNC / I2S2_LRCK
S51	HDA_SDO / I2S2_SDOUT
S52	HDA_SDI / I2S2_SDIN
S53	HDA_CK / I2S2_CK
S54	SATA_ACT#
S55	USB5_EN_OC#
S56	ESPI_IO_2
S57	ESPI_IO_3
S58	ESPI_RESET#
S59	USB5+
S60	USB5-
S61	GND
S62	USB3_SSTX+
S63	USB3_SSTX-
S64	GND
S65	USB3_SSRX+
S66	USB3_SSRX-
S67	GND
S68	USB3+
S69	USB3-
S70	GND
S71	USB2_SSTX+
S72	USB2_SSTX-
S73	GND
S74	USB2_SSRX+

P-PIN	Primary (Top) Side	S-Pin	Secondary (Bottom) Side
P74	USB3_EN_OC#	S75	USB2_SSRX-
	Key		***Key***
P75	PCIE_A_RST#	S76	PCIE_B_RST#
P76	USB4_EN_OC#	S77	PCIE_C_RST#
P77	RSVD	S78	PCIE_C_RX+
P78	RSVD	S79	PCIE_C_RX-
P79	GND	S80	GND
P80	PCIE_C_REFCK+	S81	PCIE_C_TX+
P81	PCIE_C_REFCK-	S82	PCIE_C_TX-
P82	GND	S83	GND
P83	PCIE_A_REFCK+	S84	PCIE_B_REFCK+
P84	PCIE_A_REFCK-	S85	PCIE_B_REFCK-
P85	GND	S86	GND
P86	PCIE_A_RX+	S87	PCIE_B_RX+
P87	PCIE_A_RX-	S88	PCIE_B_RX-
P88	GND	S89	GND
P89	PCIE_A_TX+	S90	PCIE_B_TX+
P90	PCIE_A_TX-	S91	PCIE_B_TX-
P91	GND	S92	GND
P92	HDMI_D2+ / DP1_LANE0+	S93	DP0_LANE0+
P93	HDMI_D2- / DP1_LANE0-	S94	DP0_LANE0-
P94	GND	S95	DP0_AUX_SEL
P95	HDMI_D1+ / DP1_LANE1+	S96	DP0_LANE1+
P96	HDMI_D1- / DP1_LANE1-	S97	DP0_LANE1-
P97	GND	S98	DP0_HPD
P98	HDMI_D0+ / DP1_LANE2+	S99	DP0_LANE2+
P99	HDMI_D0- / DP1_LANE2-	S100	DP0_LANE2-
P100	GND	S101	GND
P101	HDMI_CK+ / DP1_LANE3+	S102	DP0_LANE3+
P102	HDMI_CK- / DP1_LANE3-	S103	DP0_LANE3-
P103	GND	S104	USB3_OTG_ID
P104	HDMI_HPD / DP1_HPD	S105	DP0_AUX+
P105	HDMI_CTRL_CK / DP1_AUX+	S106	DP0_AUX-
P106	HDMI_CTRL_DAT / DP1_AUX-	S107	LCD1_BKLT_EN
P107	DP1_AUX_SEL	S108	LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+
P108	GPIO0 / CAM0_PWR#	S109	LVDS1_CK- / eDP1_AUX- / DSI1_CLK-
P109	GPIO1 / CAM1_PWR#	S110	GND

P-PIN	Primary (Top) Side
P110	GPIO2 / CAM0_RST#
P111	GPIO3 / CAM1_RST#
P112	GPIO4 / HDA_RST#
P113	GPIO5 / PWM_OUT
P114	GPIO6 / TACHIN
P115	GPIO7
P116	GPIO8
P117	GPIO9
P118	GPIO10
P119	GPIO11
P120	GND
P121	I2C_PM_CK
P122	I2C_PM_DAT
P123	BOOT_SEL0#
P124	BOOT_SEL1#
P125	BOOT_SEL2#
P126	RESET_OUT#
P127	RESET_IN#
P128	POWER_BTN#
P129	SER0_TX
P130	SER0_RX
P131	SER0_RTS#
P132	SER0_CTS#
P133	GND
P134	SER1_TX
P135	SER1_RX
P136	SER2_TX
P137	SER2_RX
P138	SER2_RTS#
P139	SER2_CTS#
P140	SER3_TX
P141	SER3_RX
P142	GND
P143	CAN0_TX
P144	CAN0_RX
P145	CAN1_TX
P146	CAN1_RX
P147	VDD_IN
P148	VDD_IN

S-Pin	Secondary (Bottom) Side
S111	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+
S112	LVDS1_0- / eDP1_TX0- / DSI1_D0-
S113	eDP1_HPD
S114	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+
S115	LVDS1_1- / eDP1_TX1- / DSI1_D1-
S116	LCD1_VDD_EN
S117	LVDS1_2+ / eDP1_TX2+ / DSI1_D2+
S118	LVDS1_2- / eDP1_TX2- / DSI1_D2-
S119	GND
S120	LVDS1_3+ / eDP1_TX3+ / DSI1_D3+
S121	LVDS1_3- / eDP1_TX3- / DSI1_D3-
S122	LCD1_BKLT_PWM
S123	RSVD
S124	GND
S125	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+
S126	LVDS0_0- / eDP0_TX0- / DSI0_D0-
S127	LCD0_BKLT_EN
S128	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+
S129	LVDS0_1- / eDP0_TX1- / DSI0_D1-
S130	GND
S131	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+
S132	LVDS0_2- / eDP0_TX2- / DSI0_D2-
S133	LCD0_VDD_EN
S134	LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+
S135	LVDS0_CK- / eDP0_AUX- / DSI0_CLK-
S136	GND
S137	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+
S138	LVDS0_3- / eDP0_TX3- / DSI0_D3-
S139	I2C_LCD_CK
S140	I2C_LCD_DAT
S141	LCD0_BKLT_PWM
S142	RSVD
S143	GND
S144	eDP0_HPD
S145	WDT_TIME_OUT#
S146	PCIE_WAKE#
S147	VDD_RTC
S148	LID#
S149	SLEEP#

P-PIN	Primary (Top) Side
P149	VDD_IN
P150	VDD_IN
P151	VDD_IN
P152	VDD_IN
P153	VDD_IN
P154	VDD_IN
P155	VDD_IN
P156	VDD_IN

S-Pin	Secondary (Bottom) Side
S150	VIN_PWR_BAD#
S151	CHARGING#
S152	CHARGER_PRSNT#
S153	CARRIER_STBY#
S154	CARRIER_PWR_ON
S155	FORCE_RECOV#
S156	BATLOW#
S157	TEST#
S158	GND

Note: Shielding should be provided on the carrier board close to the Pins S1 and S75 as differential pairs need ground or static signals right and left.

6 MECHANICAL DEFINITIONS

6.1 Carrier Connector

The Carrier board connector is a 314 pin 0.5mm pitch right angle part designed for use with 1.2mm thick mating PCBs with the appropriate edge finger pattern. The connector is commonly used for MXM3 graphics cards. The SMARC Module uses the connector in a way quite different from the MXM3 usage.

Vendor	Vendor P/N	Stack Height	Body Height	Contact Plating	Pin Style	Body Color	Notes
Foxconn	AS0B821-S43B - *H	1.5mm	4.3mm	Flash	Std	Black	
Foxconn	AS0B821-S43N - *H	1.5mm	4.3mm	Flash	Std	Ivory	
Foxconn	AS0B826-S43B - *H	1.5mm	4.3mm	10 u-in	Std	Black	
Foxconn	AS0B826-S43N - *H	1.5mm	4.3mm	10 u-in	Std	Ivory	
JAE	MM70-314B2-1-R500	1.5mm	4.3mm	0.1 u-meter	Std	Black	
Aces	91781-314 2 8-001	2.7mm	5.2mm	3 u-in	Std	Black	
Foxconn	AS0B821-S55B - *H	2.7mm	5.5mm	Flash	Std	Black	
Foxconn	AS0B821-S55N - *H	2.7mm	5.5mm	Flash	Std	Ivory	
Foxconn	AS0B826-S55B - *H	2.7mm	5.5mm	10 u-in	Std	Black	
Foxconn	AS0B826-S55N - *H	2.7mm	5.5mm	10 u-in	Std	Ivory	
Speedtech	B35P101-02121-H	2.76mm	5.2mm	Flash	Std	Black	
Speedtech	B35P101-02021-H	2.76mm	5.2mm	Flash	Std	Tan	
Speedtech	B35P101-02122-H	2.76mm	5.2mm	10 u-in	Std	Black	
Speedtech	B35P101-02022-H	2.76mm	5.2mm	10 u-in	Std	Tan	
Speedtech	B35P101-02123-H	2.76mm	5.2mm	15 u-in	Std	Black	
Speedtech	B35P101-02023-H	2.76mm	5.2mm	15 u-in	Std	Tan	
Foxconn	AS0B821-S78B - *H	5.0mm	7.8mm	Flash	Std	Black	
Foxconn	AS0B821-S78N - *H	5.0mm	7.8mm	Flash	Std	Ivory	
Foxconn	AS0B826-S78B - *H	5.0mm	7.8mm	10 u-in	Std	Black	
Foxconn	AS0B826-S78N - *H	5.0mm	7.8mm	10 u-in	Std	Ivory	
Yamaichi	CN113-314-2001	5.0mm	7.8mm	0.3 u-meter	Std	Black	Automotive Grade
Speedtech	B35P101-01133-H	5.06mm	7.5mm	15 u-in	Std	Black	
Speedtech	B35P101-03133-H	5.06mm	7.5mm	15 u-in	Std	Black	

Other, taller stack heights ***may*** be available from these and other vendors. Stack heights as tall as 11mm are shown on the Aces web site.

Note: Many of the vendor drawings for the connectors listed above show a PCB footprint pattern for use with an MXM3 graphics card. This footprint, and the associated pin numbering, is not suitable for SMARC use. The MXM3 standard gangs large groups of pins together to provide ~80W capable power paths needed for X86 graphics cards. The SMARC module “ungangs” these pins to allow more signal pins. Footprint and pin numbering information for application of this 314 pin connector to SMARC is given in the sections below.

6.2 Module and Carrier Connector Pin Numbering Convention

The Module pins are designated as P1 – P156 on the Module Primary (Top) side, and S1 – S158 on the Module Secondary (Bottom) side. There is a total of 314 pins on the Module. The connector is sometimes identified as a 321 pin connector, but 7 pins are lost to the key (4 on the primary side and 3 on secondary side).

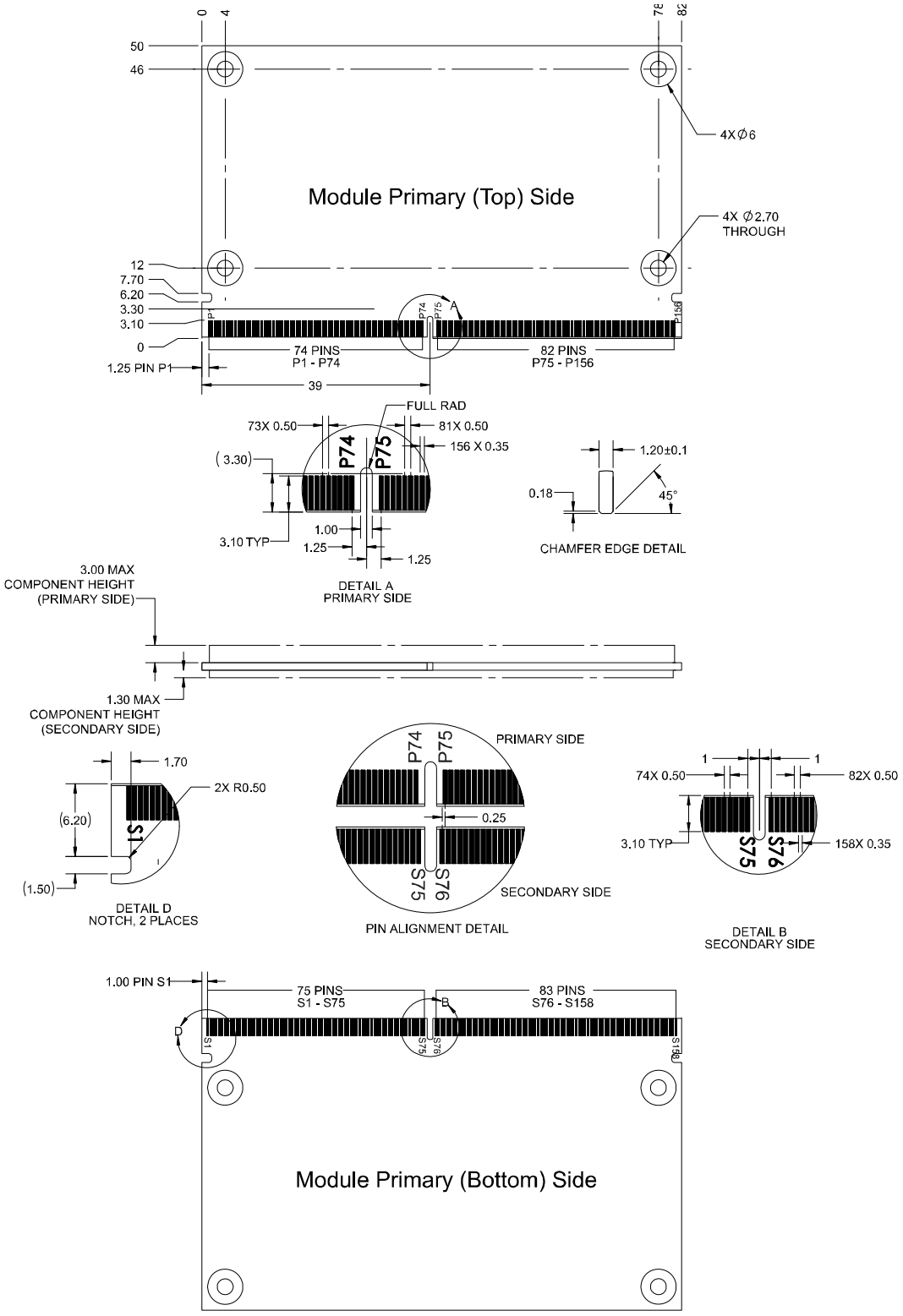
The Secondary (Bottom) side faces the Carrier board when a normal or standard Carrier connector is used. Some connector vendors offer “reverse” pin-out connectors, which effectively flip the Module over such that the Module Primary side would face the Carrier board.

The SMARC Module pins are deliberately numbered as P1 – P156 and S1 – S158 for clarity and to differentiate the SMARC Module from MXM3 graphics modules, which use the same connector but use the pins for very different functions. MXM3 cards and MXM3 baseboard connectors use a different pin numbering scheme.

6.3 Module Outline – 82mm x 50mm Module

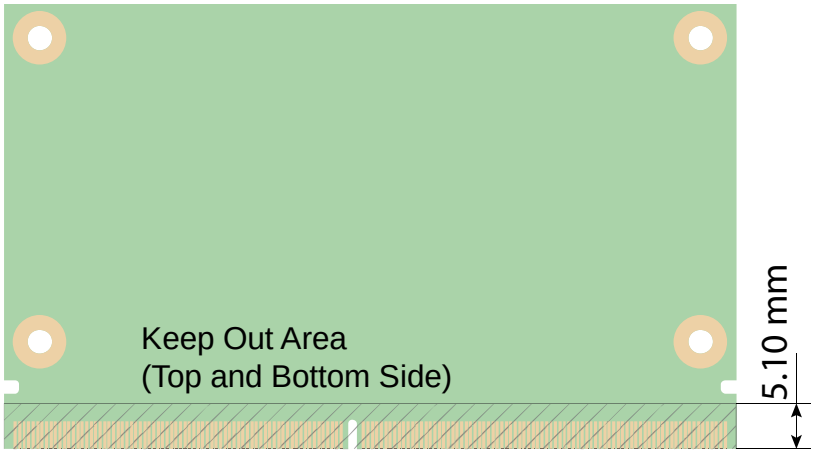
The Figure 1 on the following page details the 82mm x 50mm Module mechanical attributes, including the pin numbering and edge finger pattern.

Figure 1: 82mm x 50mm Module Outline



It is recommended that Module components be kept away from the edge fingers, on the top and bottom sides, per the following figure:

Figure 2: Module Edge Finger Keep Out Area (82mm x 50mm Module)



6.4 Module Outline – 82mm x 80mm Module

The 82mm x 80mm Module is shown in the Figure 3 below. The PCB edge finger pattern and spacing details relative to the board edges and lower mounting holes are the same as for the 82mm x 50mm case, and are not repeated here.

Figure 3: 82mm x 80mm Module Outline

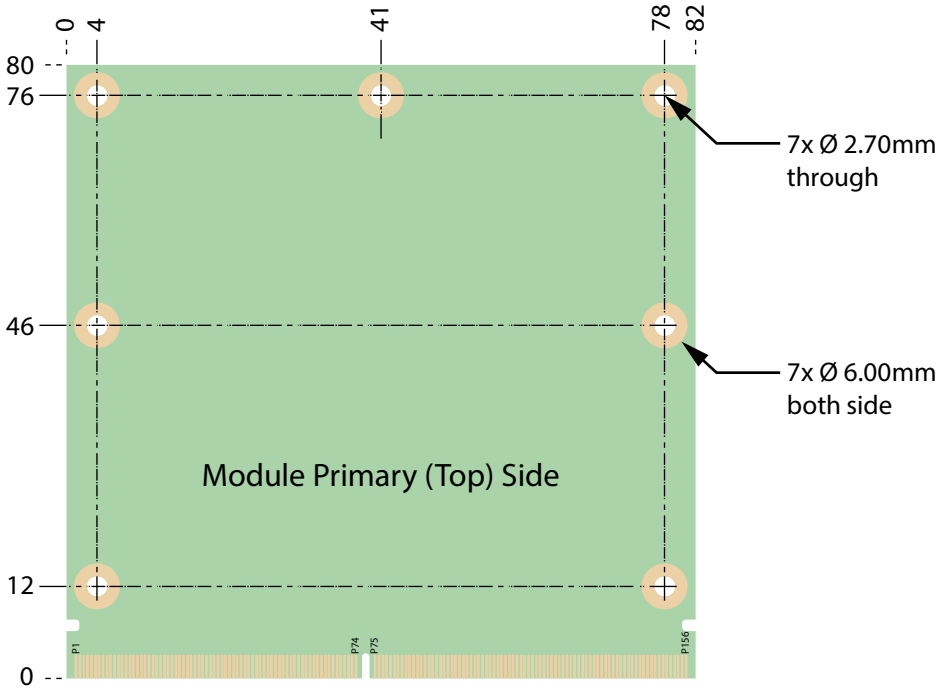
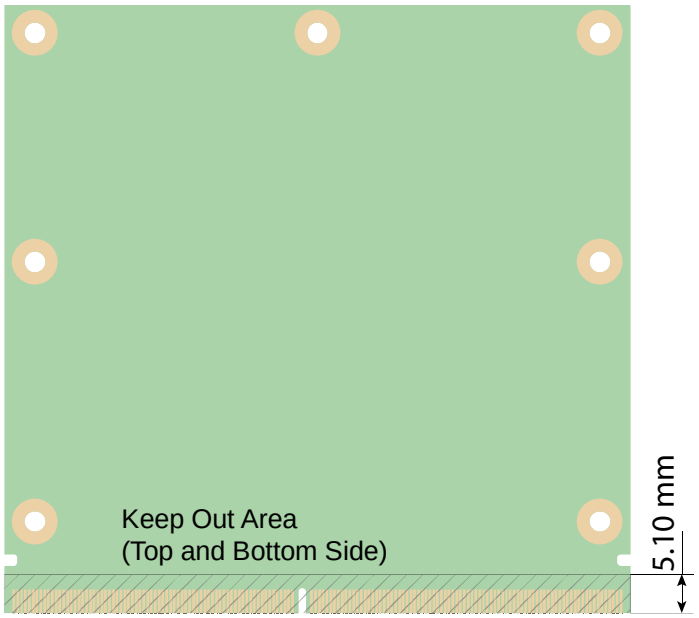


Figure 4: Module Edge Finger Keep Out Area (82mm x 80mm Module)



6.4.1 RF Connector Placement

If onboard wireless technologies are provided the required high frequency antenna connectors ***shall*** be placed at the described positions on the top side of the modules. If no wireless technologies are provided this position ***may*** be used for other components.

u.FL male connectors ***should*** be used on the modules. This are miniature RF connectors with an impedance of 50 ohm for antenna applications. U.FL connectors are commonly used for Wi-Fi or GPS in space critical applications. The mated connection is only 2.5 mm high and only requires 3 mm² of board space. u.FL connectors are patented by Hirose but there are many other suppliers offering this connectors.

Figure 5: u.FL connector

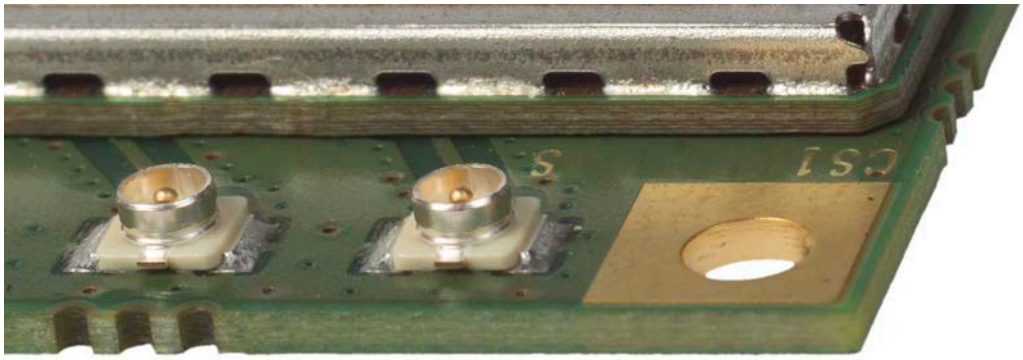


Figure 6: RF connector placement (82mm x 80mm Module)

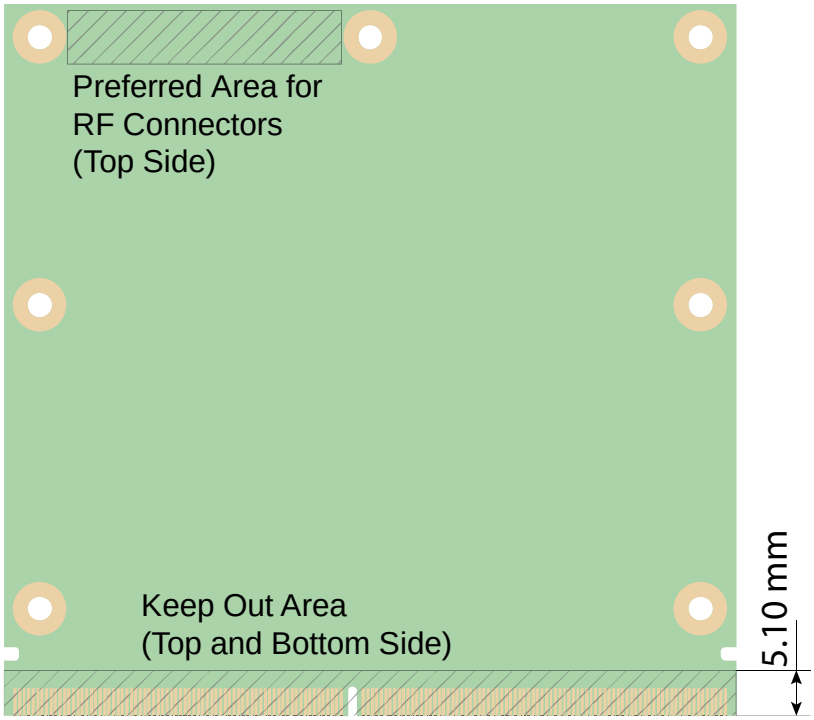
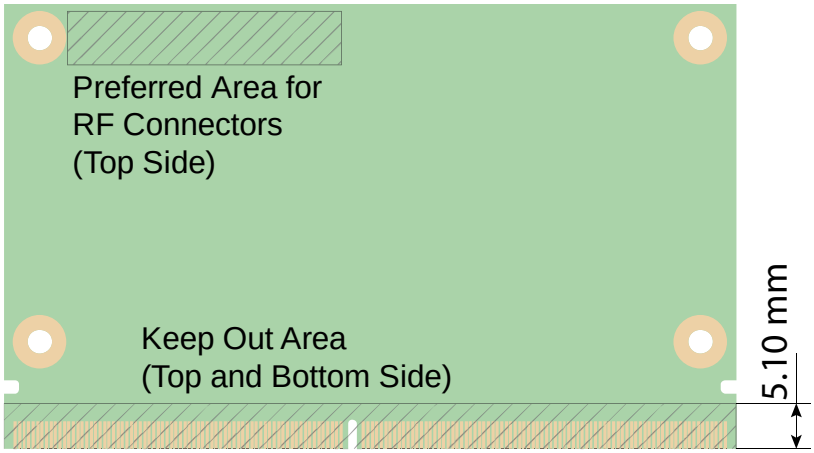


Figure 7: RF connector placement (82mm x 50mm Module)



6.5 Module ‘Z’ Height Considerations

Note from above that the component height on the Module is restricted to a maximum component height of 3mm on the Module Primary (Top) side and to 1.3mm on the Module Secondary (Bottom) side.

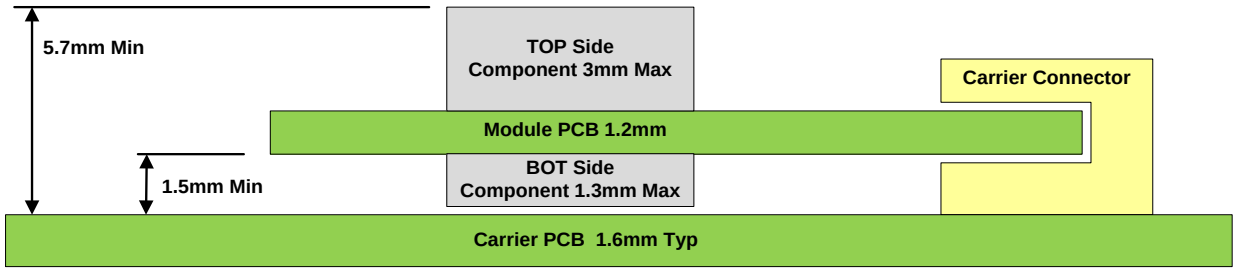
The 1.3mm Secondary side component height restriction allows the Module to be used with 1.5mm stack-height Carrier connectors. When used with 1.5mm stack height connectors, the ‘Z’ height profile from Carrier board Top side to tallest Module component is 5.7mm.

When a 1.5mm stack height Carrier board connector is used, there ***shall not*** be components on the Carrier board Top side in the Module region. Additionally, when 1.5mm stack height connectors are used, there ***should not*** be PCB traces on the Carrier top side in the Module shadow. This is to prevent possible problems with metallic Module heat sink attachment hardware that ***may*** protrude through the Module.

If Carrier board components are required in this region, then the Carrier components must be on the Carrier Bottom side, or a taller Module – to – Carrier connector ***may*** be used. Stack heights of 2.7mm, 3mm, 5mm and up are available.

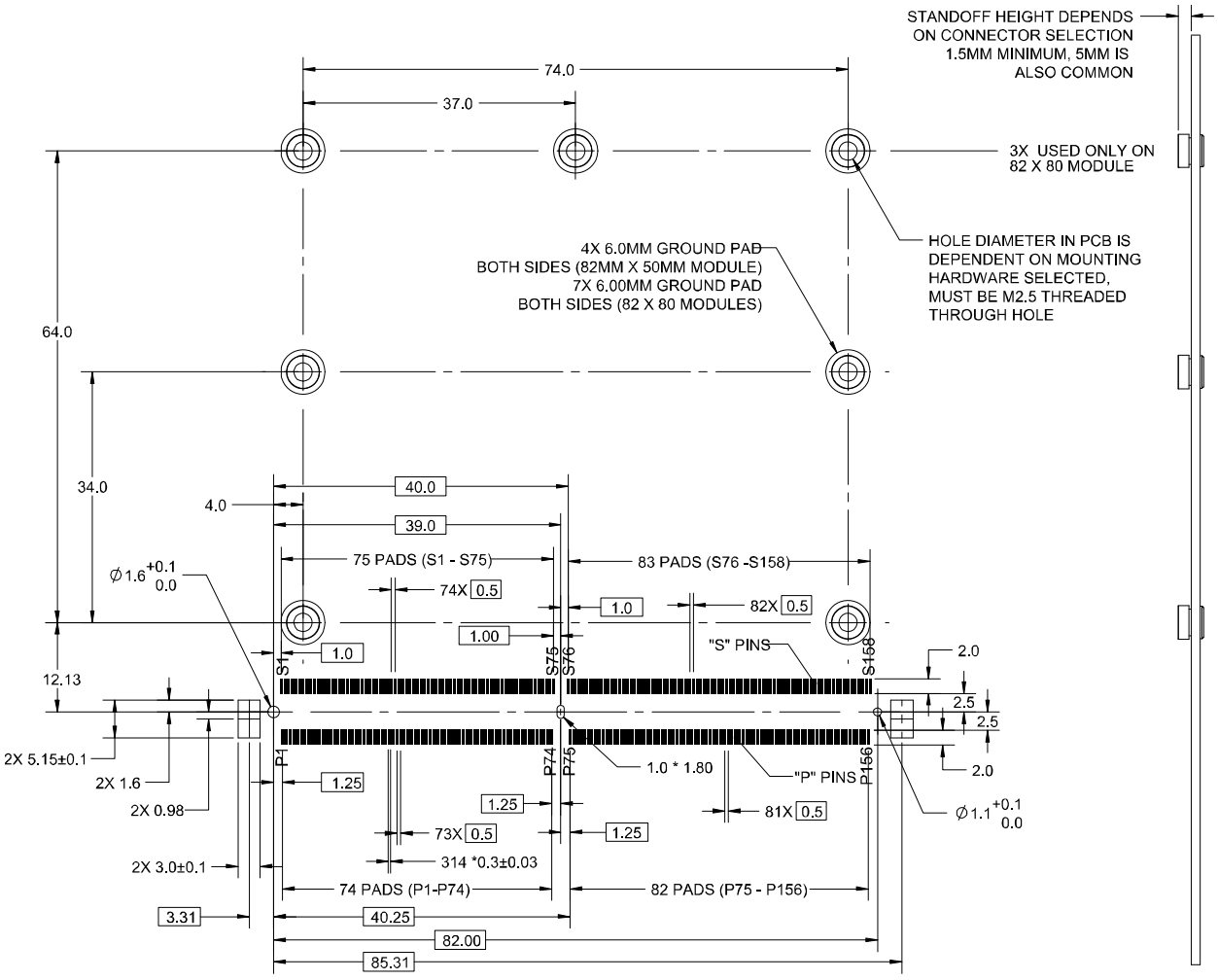
Not shown in the Figure 8 below are any thermal dissipation components (heat sinks, heat spreaders, etc) nor is fastening hardware (standoffs, spacers, screws, washers, etc) shown. The dimensions of those components must of course be considered in a system design.

Figure 8: Module Minimum 'Z' Height



6.6 Carrier Board Connector PCB Footprint

Figure 9: Carrier Board Connector PCB Footprint



Note: The pin numbering shown here is different from the pin numbering used in an MXM3 application. In an SMARC application, all 314 pins of the connector are used individually. The MXM3 power ganging is not used.

Note: The hole diameter for the 4 holes (82mm x 50mm Module) or 7 holes (82mm x 80mm Module) depends on the spacer hardware selection. See the section 6.7 ‘Module and Carrier Board Mounting Holes – GND Connection’ below for more information on this.

6.7 Module and Carrier Board Mounting Holes – GND Connection

It ***shall*** be possible to tie all Module and Carrier board mounting holes to GND. The holes ***should*** be tied directly to the GND planes, although Module and Carrier designers ***may*** optionally make the mounting hole GND connections through passive parts, allowing the mounting holes to be isolated from GND if they feel it necessary.

6.8 Carrier Board Standoffs

Standoffs secured to the Carrier board are expected. The standoffs are to be used with M2.5 hardware. Most implementations will use Carrier board standoffs that have M2.5 threads (as opposed to clearance holes). A short M2.5 screw and washer, inserted from the Module top side, secures the Module to the Carrier board threaded standoff.

6.9 Thermal Attachment Points

Attachment points for thermal heat sinks and thermal dissipaters, if needed, are Module design dependent. Thermal hardware ***should*** be attached to the Module using attachment points other than the Module mounting holes (4 mounting holes for the 82mm x 50mm and 7 mounting holes for the 82mm x 80mm Module). The Module mounting holes ***should*** be clear for securing the Module to the Carrier.

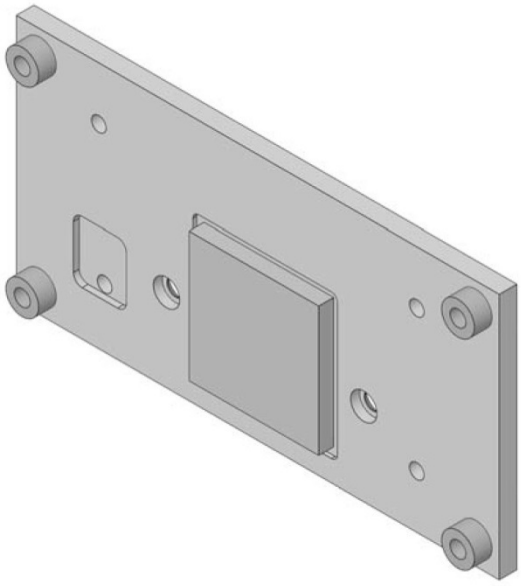
Having thermal attachment points separate from the Module mounting holes allows the thermal solution to be shipped with the Module, attached to the Module with thermal interface materials applied, and avoids the disassembly of the thermal interface materials when the end-user places the Module into their system. The Module mounting holes ***may*** be used as supplemental thermal attachment points.

6.10 Heat Spreader – 82mm x 50mm Module

A standard heat-spreader plate for use with the SMARC 82mm x 50mm form factor is described below. A standard heat spreader plate definition allows the customer to use a Module from multiple vendors, and the details of the thermal interface to the Module ICs – which can be tricky - becomes the Module designer's problem.

The heat spreader plate is sized at 82mm x 42mm x 3mm, and sits 3mm above the SMARC Module. The heat spreader plate 'Y' dimension is deliberately set at 42mm and not 50mm, to allow the plate to clear the SMARC MXM3 connector. The plate is shown in the Figure 10 below.

Figure 10: Heat Spreader Isometric View



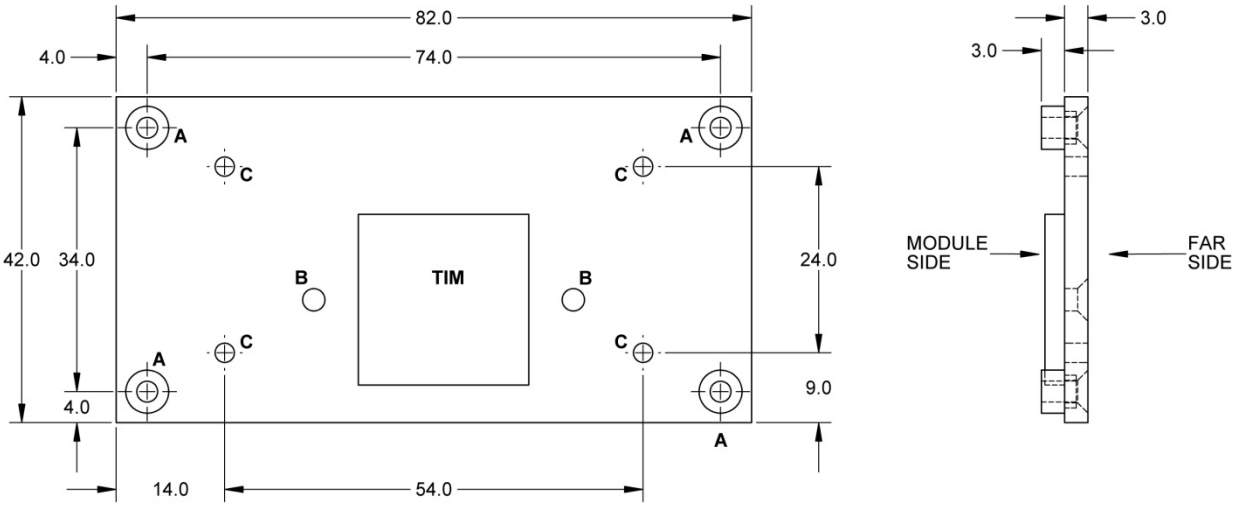
The internal square in the Figure 10 above is a thermally conductive and mechanically compliant Thermal Interface Material (or "TIM"). The exact X-Y position and Z thickness details of the TIM vary from design to design.

The two holes immediately adjacent to the TIM serve to secure the PCB in the SOC area and compress the TIM.

The four interior holes that are further from the center allow a heat sink to be attached to the heat spreader plate, or they can be used to secure the heat spreader plate to a chassis wall that serves as a heat sink.

Dimensions and further details ***may*** be found in the Figure 11 'Heat Spreader Plan View' on the following page.

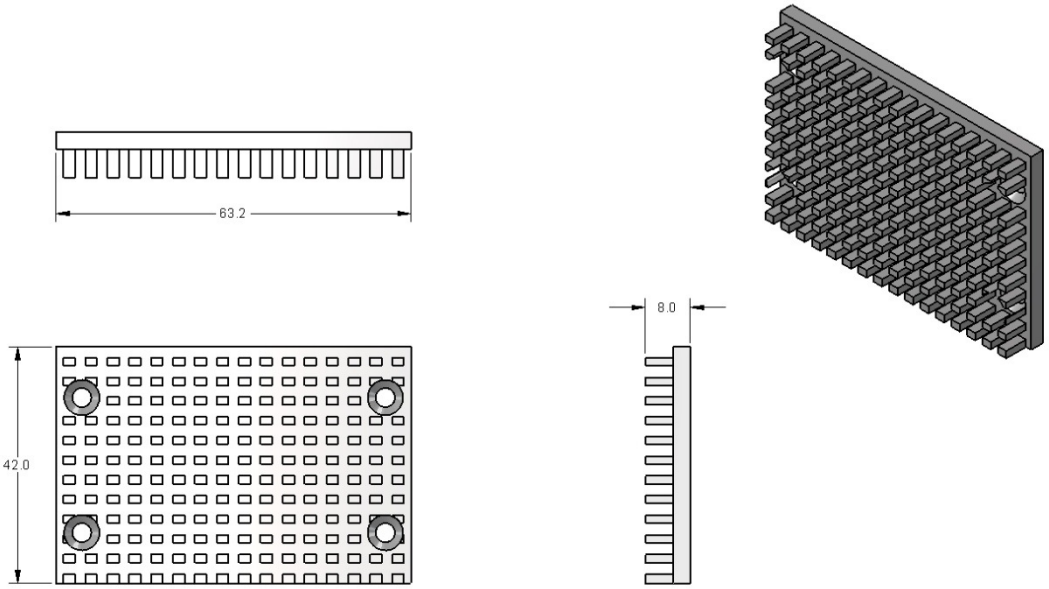
Figure 11: Heat Spreader Plan View



Dimensions in the figure above are in millimeters. “TIM” stands for “Thermal Interface Material”. The TIM takes up the small gap between the SOC top and the Module - facing side of the heat spreader.

Hole Reference	Description	Size
A	SMARC Module corner mounting holes Spacing determined by SMARC specification for 82mm x 50mm Modules. Typically these holes have 3mm length press fit or swaged clearance standoffs on the Module side. These holes are typically countersunk on the far side of the plate, to allow the heat spreader plate to be flush with a secondary heat sink.	Hole size depends on standoffs used. Standoff diameter must be compatible with SMARC Module mounting hole pad and hole size (6.0mm pads, 2.7mm holes on the Module). The holes and standoffs are for use with M2.5 screw hardware. The far side of these holes are counter-sunk to allow the attachment screw to be flush with the far side heat spreader surface.
B	Design – specific attachment points. The X-Y position, size and finish details of these holes ***may*** vary between designs.	Varies, design dependent The far side of these holes are counter-sunk to allow the attachment screw to be flush with the far side heat spreader surface.
C	Fixed location holes to allow the attachment of a heat sink to the heat spreader, or to allow the heat spreader to be secured to a chassis wall that can serve as a heat sink.	M3 threaded holes

Figure 12: Heat Sink Attachment Option



This figure shows an optional heat sink that can be added on to the heat spreader plate. Some situations ***may*** require a taller heat sink and / or one with an embedded fan. The four holes in the heat sink above are used with M3 flat head screws. The screws engage the 'C' holes in the heat spreader plate in Figure 11 'Heat Spreader Plan View' on the previous page. A relatively large, thin TIM is required between the heat spreader plate "Far Side" and the flat surface of the heat sink.

The heat sink Y dimension matches the 42mm Y dimension of the heat spreader plate. The X dimension of the heat sink is less, at 63.2 mm, than the 82 mm length of the heat spreader plate. This is to allow the heat sink to clear the four Module corner holes (the 'A' holes in Figure 11 'Heat Spreader Plan View'). The heat sink Z dimension can vary according to the thermal situation at hand.

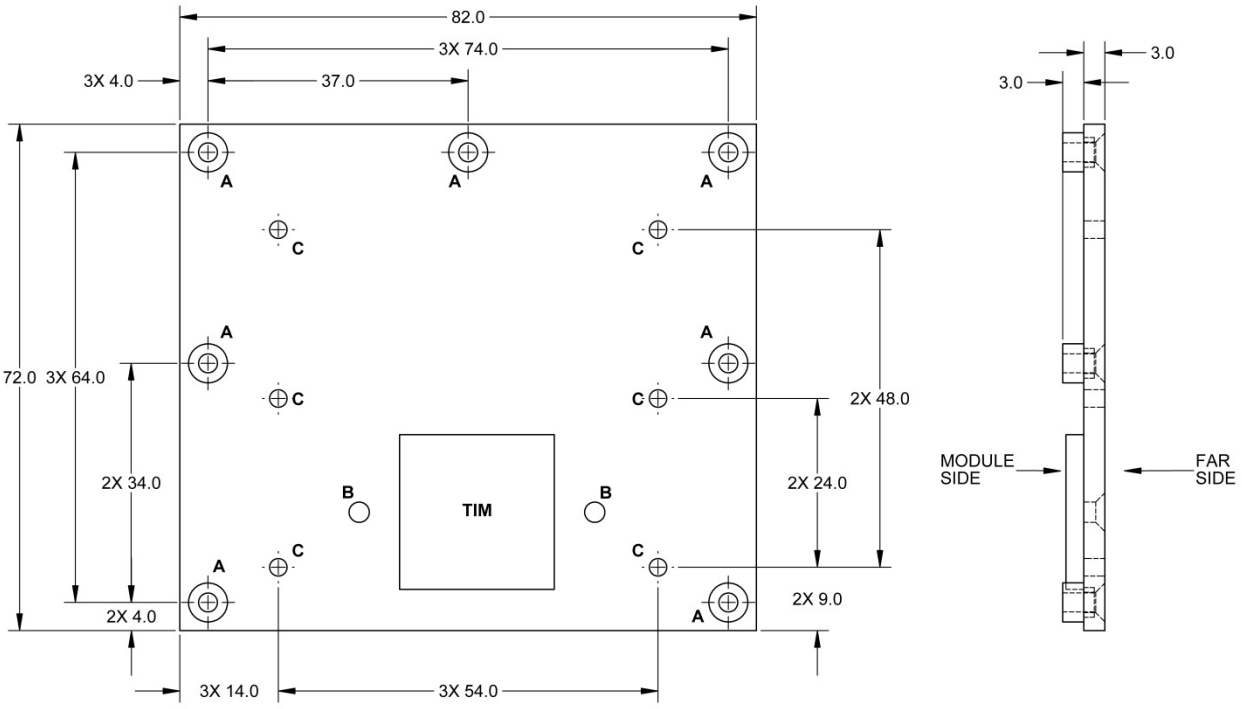
Alternatively, the system enclosure wall ***may*** be used as the heat sink. In this case, the heat spreader plate is secured to the enclosure wall via the four 'C' holes shown in Figure 11 'Heat Spreader Plan View' on the previous page. A large, thin TIM is then required between the heat spreader plate "Far Side" and the enclosure wall.

6.11 Heat Spreader – 82mm x 80mm Module

The heat spreader for an 82mm x 80mm Module is similar to the heat spreader for the 82mm x 50mm Module, but is extended upward by 30mm and appropriate additional holes are provided. The ‘A’ and ‘C’ hole drill details are the same as the ‘A’ and ‘C’ holes on the heat spreader for the 82mm x 50mm Module.

The TIM and the B holes are not fixed, and ***may*** be in locations other than what is shown in Figure 13.

Figure 13: Heat Spreader - 82mm x 80mm Module



7 MODULE POWER

7.1 Input Voltage / Main Power Rail

The Module input power voltage is brought in on the ten VDD_IN pins and returned through the numerous GND pins on the connector.

A Module ***shall*** withstand an indefinite exposure to an applied VDD_IN that ***may*** vary over the 3.0V to 5.25V range, without damage.

A Module ***should*** operate over the entire VDD_IN range of 3.0V to 5.25V.

Modules that use higher wattage SOCs ***may*** be designed to operate with a fixed 5V supply (4.75V to 5.25V).

Modules that are designed for rock-bottom cost and that use low power SOCs ***may*** be designed to operate with a fixed 3.3V supply (3.1V to 3.4V). They ***shall not*** be damaged in any way by exposure to the allowable VDD_IN range of 3.0 to 5.25V.

Ten pins are allocated to VDD_IN. The connector pin current rating is 0.5A per pin. This works out to 5A total for the 10 pins. At the lowest allowed Module input voltage of 3.0V, this would allow up to 15W of electrical power to be brought in (with no de-rating on the connector current capability). With a 40% connector current de-rating, up to 9W ***may*** be brought in at 3.0V.

If the fixed 5V input option is used, then 25W ***may*** be brought in over the 10 power pins (no de-rating). With a 40% connector de-rating, 15W are allowed to be brought in at 5V

As a practical matter, ARM most Module designs are expected to be 6W or less. X86 designs are expected to be in the 5W to 12W range, depending on the CPU SKU.

7.2 No Separate Standby Voltage

There is no separate voltage rail for standby power, other than the very low current (optional) RTC voltage rail. All Module operating and standby power comes from the single set of VDD_IN pins. This suits battery power sources well, and is also easy to use with non-battery sources.

7.3 RTC Voltage Rail

RTC backup power ***may*** brought in on the VDD_RTC rail. The RTC consumption is typically 15 microA or less. The allowable VDD_RTC voltage range ***shall*** be 2.0V to 3.25V. The VDD_RTC rail ***may*** be sourced from a Carrier based Lithium cell or Super Cap, or it ***may*** be left open if the RTC backup functions are not required. The Module ***shall*** be able to boot without an external VDD_RTC voltage source.

Important: Lithium cells must be protected against charging by reverse currents, with a series Schottky diode and resistor. It is impractical to have the series diode on the Module, as this complicates the use of Super Caps (they need to be charged, over the Module VDD_RTC pin).

Lithium cells, if used, ***shall*** be protected against charging by a Carrier Schottky diode. The diode is placed in series with the positive battery terminal. The diode anode is on the battery side, and the cathode on the Module VDD_RTC side.

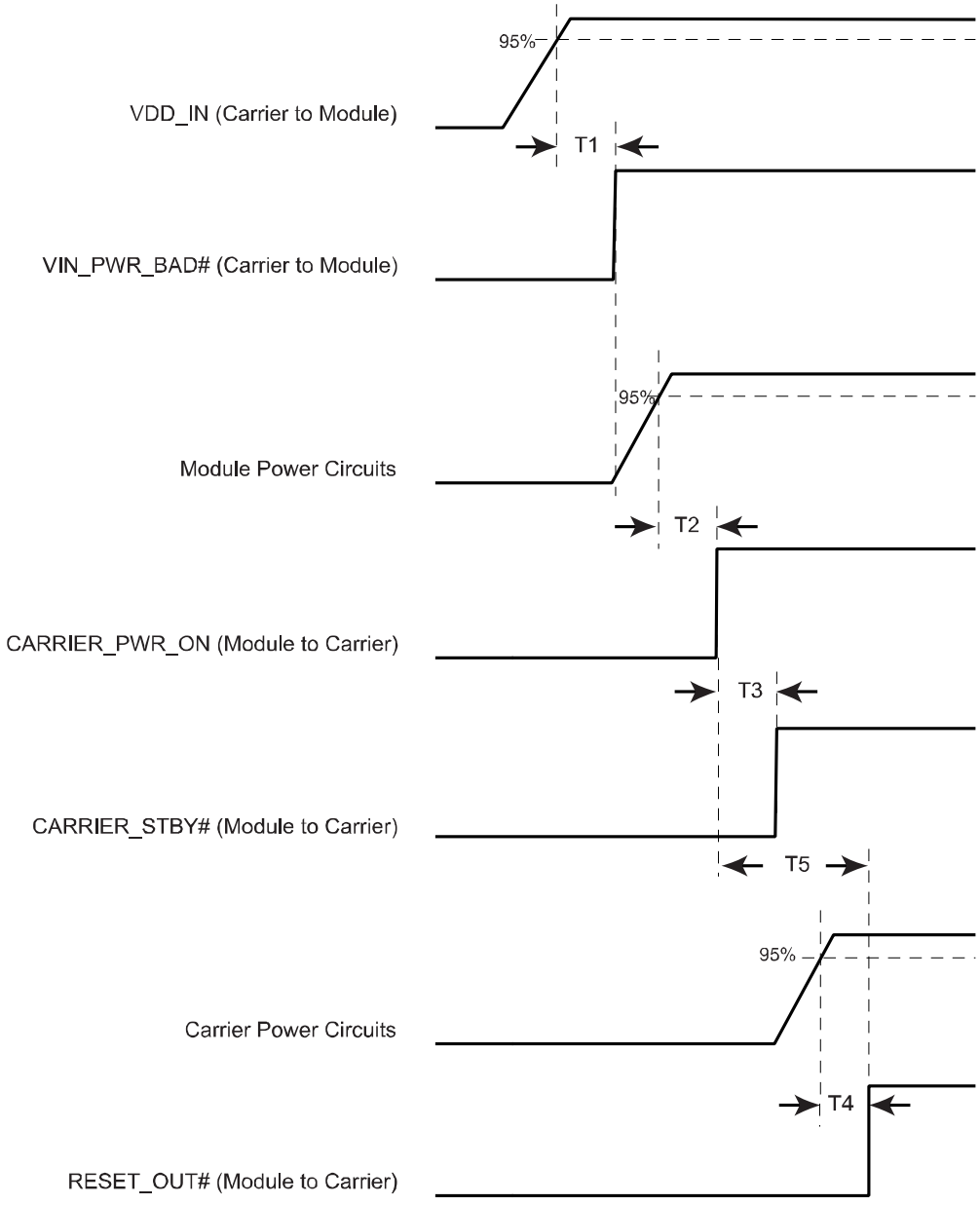
Note that if a Super cap is used, current ***may*** flow out of the Module VDD_RTC rail to charge the Super Cap.

7.4 Power Sequencing

The Module signal CARRIER_PWR_ON exists to ensure that the Module is powered before the main body of Carrier circuits (those outside the power and power control path on the Carrier). The main body of Carrier board circuits ***should not*** be powered until the Module asserts the CARRIER_PWR_ON signal as a high. Module hardware ***should*** assert CARRIER_PWR_ON when all Module supplies necessary for Module booting are up. The Module ***should*** continue to assert signal CARRIER_RESET_OUT# after the release of CARRIER_PWR_ON, for a period sufficient (100ms to 500ms) to allow Carrier power circuits to come up.

Only one single supply voltage rail is used for the module. There are no timing relations between this module supply rail VDD_IN and the optional VDD_RTC.

Figure 14: Power On Sequencing



Item	Description	Value
T1	VDD_IN stable to VIN_PWR_BAD# rise	≥ 0 ms
T2	Module supplies necessary for Module booting are up to CARRIER_PWR_ON rise	≥ 0 ms
T3	CARRIER_PWR_ON to CARRIER_STBY# timing	≥ 0 ms
T4	Carrier power circuits are up to RESET_OUT# rise	≥ 0 ms
T5	CARRIER_PWR_ON to CARRIER_RESET_OUT# timing	100 .. 500 ms

7.4.1 x86 Power Management

The power management of x86 systems typically utilizes the signals SUS_S5# and SUS_S3# to indicate the sleep states and to control the ATX power supply. SMARC supports only single voltage supply and no ATX power supply; therefore these signals can only be used to indicate, if the module is in one of the sleep states.

For S3 state the SMARC signal CARRIER_STBY# ***should*** be utilized

For S5 states the SMARC signal CARRIER_PWR_ON ***should*** be utilized, but the CARRIER_PWR_ON functionality to avoid back driving ***shall*** be still maintained.

SUS_S3# CPU Signal

Indicates system is in Suspend to RAM state.

ACPI S3 State "Suspend to RAM"

The CPU is not executing instructions, is not ready to execute instructions, does not maintain its registers and does not maintain cache. The OS must flush dirty pages from the cache when S3 is entered. Devices able to support S3 and are enabled for resuming, may resume the system. Power supply state is off, system RAM is refreshed. External peripherals (keyboard, mouse) may or may not be able to resume the system, depending on their host controller.

SUS_S5# CPU Signal

Indicates system is in Soft Off state.

ACPI S5 State "Soft-Off"

All hardware is in the off state and maintains no context. CMOS is maintained, as in S4. The power supply is in off state. Power may be mechanically removed without ill effect.

7.5 System Power Domains

It is useful to describe an SMARC system as being divided into a hierarchy of three power domains:

1) Battery Charger power domain
2) SMARC Module power domain
3) Carrier Circuits power domain

The Battery Charger domain includes circuits that are active whenever either charger input power and / or battery power are available. These circuits ***may*** include power supply supervisor(s), battery chargers, fuel gauges and, depending on the battery configuration, switching power section(s) to step down a high incoming battery voltage.

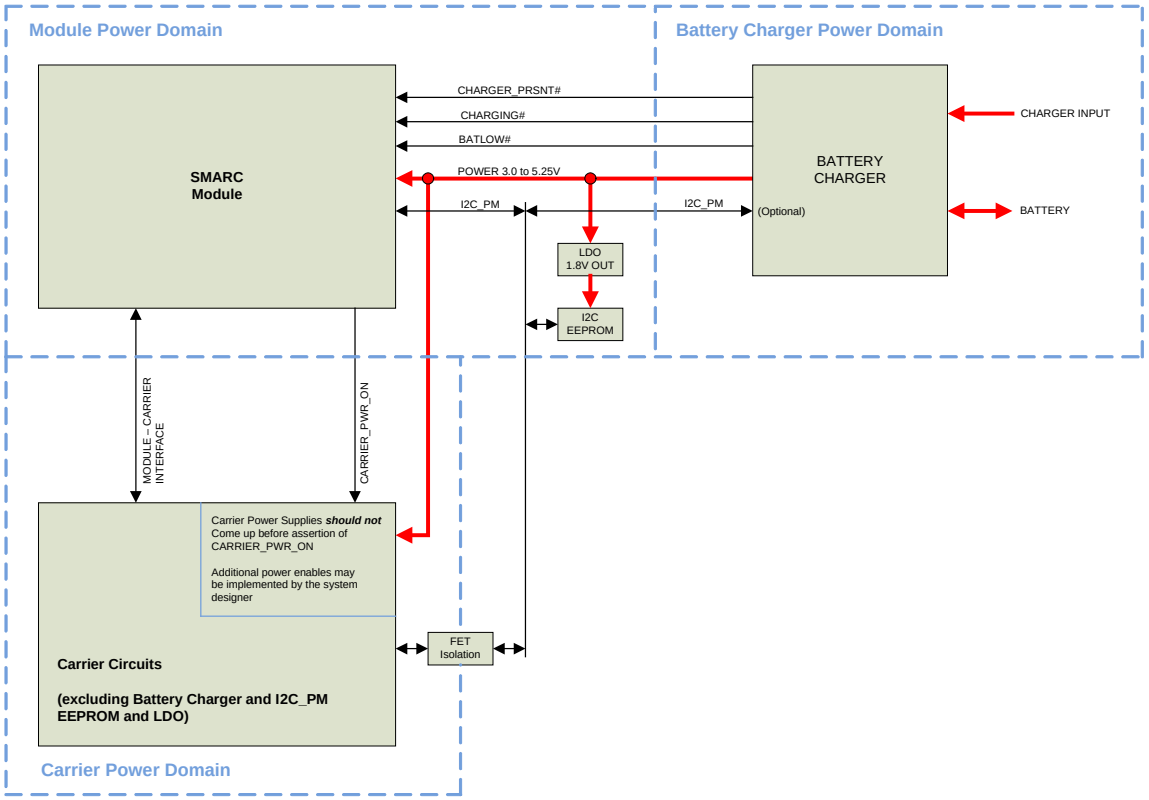
The SMARC Module domain includes the SMARC module and ***may*** include a serial EEPROM on the Carrier, connected to the I2C_PM I2C bus in the Module power domain, allowing Module software to read Carrier board parameters.

The Carrier Circuits domain includes “everything else” (and does not include items from the Battery Charger and Module domain, even though they ***may*** be mounted on the Carrier).

This is illustrated in the Figure 15 below.

Note: Not shown in the Figure 15 is the additional, optional, fine grain power control that the Module ***may*** exert on the Carrier board, using design specific I/O. The power control I/O ***may*** be implemented via I2C I/O expanders (e.g. Texas Instruments TCA9554 or TC7408), or by other means.

Figure 15: System Power Domains



8 MODULE AND CARRIER SERIAL EEPROMS

SMARC Modules ***should*** include an I2C serial EEPROM on the Module I2C_GP bus. The device used ***should*** be an Atmel 24C32 or equivalent. The device ***shall*** operate at 1.8V. The Module serial EEPROM ***should*** be placed at I2C slave addresses A2 A1 A0 set to 0 (I2C slave address 50 hex, 7 bit address format or A0 / A1 hex, 8 bit format) (recall that for I2C EEPROMs, address bits A6 A5 A4 A3 are set to binary 0101 convention).

The Module serial EEPROM is intended to retain Module parameter information, including a Module serial number. The Module serial EEPROM data structure ***should*** conform to the ***PICMG® EEEP Embedded EEPROM Specification***.

SMARC Carriers ***may*** include an I2C serial EEPROM on the I2C_PM bus, in the Module power domain. The device used ***should*** be an Atmel 24C32 or equivalent. The device ***shall*** operate at 1.8V. The Carrier serial EEPROM ***should*** be placed with I2C slave addresses A2 A1 A0 set to binary 111 (I2C slave address 57 hex, 7 bit address format or AE / AF hex, 8 bit format).

The Carrier serial EEPROM is intended to retain Carrier parameter information. The Carrier serial EEPROM data structure ***should*** conform to the ***PICMG® EEEP Embedded EEPROM Specification***.

9 APPENDIX A: LVDS LCD COLOR MAPPINGS

9.1 LVDS LCD Color Mappings

For flat panel use, parallel LCD data and control information (Red, green and blue color data; Display Enable, Vertical Synch, Horizontal Synch) are commonly serialized onto a set of LVDS differential pairs. The information is packed into frames that are 7 bits long. For 18 bit color depths, the data and control information utilize three LVDS channels (18 data bits + 3 control bits = 21 bits; hence 3 channels with 7 bit frames) plus a clock pair. For 24 bit color depths, four LVDS channels are used (24 data bits + 3 control bits + 1 unused bit = 28 bits, or 4 x 7) plus a clock pair.

The LVDS clock is transmitted as a separate LVDS pair. The LVDS clock period is 7 times longer than the pixel clock period. The LVDS clock edges are off from the 7 bit frame boundaries by 2 pixel periods.

Unfortunately, there are two different 24 bit color mappings in use. The more common one, sometimes referred to as “24 bit standard color mapping”, is not compatible with 18 bit panels, as it places the most significant RGB color data on the 4th LVDS data pair – the pair that is not used on 18 bit panels. There is a less common “24 bit / 18 bit compatible” mapping that puts the least significant color bits of the 24 bit set onto the 4th LVDS pair.

Some panels have pin straps that allow the user to select which color mapping is to be used.

The color mappings are summarized in the table below. The table includes a reference to a Texas Instruments LVDS transmitter, the SN75LVDS83B, showing the transmitter input pin names that TI lists in their sheet.

9.1.1 Single Channel LVDS LCD Color Mappings – General Information

LVDS Channel	Transmit Bit Order	18 bit Standard	24 Bit Standard	24 Bit / 18 Bit Compatible	SN75LVDS83B Pin Name
0	1	G0	G0	G2	D7
	2	R5	R5	R7	D6
	3	R4	R4	R6	D4
	4	R3	R3	R5	D3
	5	R2	R2	R4	D2
	6	R1	R1	R3	D1
	7	R0	R0	R2	D0
1	1	B1	B1	B3	D18
	2	B0	B0	B2	D15
	3	G5	G5	G7	D14
	4	G4	G4	G6	D13
	5	G3	G3	G5	D12
	6	G2	G2	G4	D9
	7	G1	G1	G3	D8
2	1	DE	DE	DE	D26
	2	VS	VS	VS	D25
	3	HS	HS	HS	D24
	4	B5	B5	B7	D22
	5	B4	B4	B6	D21
	6	B3	B3	B5	D20
	7	B2	B2	B4	D19
3	1	<not used>	<not used>	<not used>	D23
	2	<not used>	B7	B1	D17
	3	<not used>	B6	B0	D16
	4	<not used>	G7	G1	D11
	5	<not used>	G6	G0	D10
	6	<not used>	R7	R1	D5
	7	<not used>	R6	R0	D27

9.1.2 Single Channel LVDS LCD 24 Bit Standard Color Mapping – Carrier Connections

LVDS Channel	Transmit Bit Order	24 Bit Colors	Module Pin Name	SN75LVDS83B Pin Name
0	1	G0	LCD_D[8]	D7
	2	R5	LCD_D[21]	D6
	3	R4	LCD_D[20]	D4
	4	R3	LCD_D[19]	D3
	5	R2	LCD_D[18]	D2
	6	R1	LCD_D[17]	D1
	7	R0	LCD_D[16]	D0
1	1	B1	LCD_D[1]	D18
	2	B0	LCD_D[0]	D15
	3	G5	LCD_D[13]	D14
	4	G4	LCD_D[12]	D13
	5	G3	LCD_D[11]	D12
	6	G2	LCD_D[10]	D9
	7	G1	LCD_D[9]	D8
2	1	DE	LCD_DE	D26
	2	VS	LCD_VS	D25
	3	HS	LCD_HS	D24
	4	B5	LCD_D[5]	D22
	5	B4	LCD_D[4]	D21
	6	B3	LCD_D[3]	D20
	7	B2	LCD_D[2]	D19
3	1	<not used>	<not used>	D23
	2	B7	LCD_D[7]	D17
	3	B6	LCD_D[6]	D16
	4	G7	LCD_D[15]	D11
	5	G6	LCD_D[14]	D10
	6	R7	LCD_D[23]	D5
	7	R6	LCD_D[22]	D27

For a 24 bit standard color map single channel LVDS implementation, connect the Module pins to the Carrier board LVDS transmitter input pins as shown in the table above.

The LVDS transmitter clock input (pin name CLKIN on the TI SN75LVDS83B) ***should*** be driven by the Module parallel LCD interface pixel clock: the Module LCD_PCK pin.

Some LVDS transmitters, including the SN75LVDS83B, have a pin allowing the user to select which edge of the pixel clock is to be used to latch the data coming in to the LVDS transmitter. In most cases, this pin ***should*** be set for a rising edge clock latching. A resistor or jumper option allowing either edge to be used is recommended.

9.1.3 Dual Channel LVDS LCD 24 Bit Standard Color Mapping – Carrier Connections

Dual channel LVDS implementations are used to drive high resolution panels (generally, panel resolutions of 1280 x 1024 and above). In a dual channel implementation, the parallel pixel data is fed to a pair of LVDS transmitters. The pair of transmitters form two sets of LVDS streams ("dual channel"). The first set has the odd pixel information and the second set has the even pixel information. By convention, the upper left most pixel on a display is "odd", the next one on the line is "even", and so on.

A 24 bit dual channel LVDS implementation comprises 10 differential pairs: 4 pairs for odd pixel and control data; 1 pair for the LVDS clock for the odd data; 4 pairs for the even pixel data and control data, and 1 pair for the even LVDS clock.

The same 18 / 24 bit color mapping considerations described earlier in this document apply to dual channel displays. However, as dual channel displays are higher end products, they tend to be 24 bit devices, usually with the standard 24 bit color mapping.

10 APPENDIX C: DOCUMENT CHANGES

10.1 SMARC HW Specification Changes V1.1 to V2.0

Removed Interfaces

- Parallel camera interface
- Parallel Display interface
- PCI Express presence and clock request signals
- Alternate function block
- SPDIF
- eMMC
- 1 of 3 I2S

Added Interfaces

- 2nd channel LVDS
- 2nd Ethernet
- IEEE1588 trigger signals (software definable pins)
- 4th PCI Express lane
- Extra USB ports (6x USB 2.0 + 2x USB SS signals now)
- x86 power management signals
- eSPI
- DP++

Total Video Interfaces now

- 2x 24 Bit LVDS / eDP 4 channel / MIPI DSI 4 channel
- HDMI / DP++
- DP++

Other Changes

- Added RF connector option
- Changed Module EEPROM from I2C_PM to I2C_GP
- Added power sequencing details
- See detailed pinout changes is section 10.1.1 ‘Pinout Comparison’ below
- Some mandatory and optional features changed, see section 3.1 ‘Required and Optional Feature Table’ on page 12

10.1.1 Pinout Comparison

Pin	SMARC 1.1	SMARC 2.0
P1	~~PCAM_PXL_CK1~~	SMB_ALERT_1V8#
P2	GND	GND
P3	CSI1_CK+ ~~/ PCAM_D0~~	CSI1_CK+
P4	CSI1_CK- ~~/ PCAM_D1~~	CSI1_CK-
P5	~~PCAM_DE~~	GBE1_SDP
P6	~~PCAM_MCK~~	GBE0_SDP
P7	CSI1_D0+ ~~/ PCAM_D2~~	CSI1_RX0+
P8	CSI1_D0- ~~/ PCAM_D3~~	CSI1_RX0-
P9	GND	GND
P10	CSI1_D1+ ~~/ PCAM_D4~~	CSI1_RX1+
P11	CSI1_D1- ~~/ PCAM_D5~~	CSI1_RX1-
P12	GND	GND
P13	CSI1_D2+ ~~/ PCAM_D6~~	CSI1_RX2+
P14	CSI1_D2- ~~/ PCAM_D7~~	CSI1_RX2-
P15	GND	GND
P16	CSI1_D3+ ~~/ PCAM_D8~~	CSI1_RX3+
P17	CSI1_D3- ~~/ PCAM_D9~~	CSI1_RX3-
P18	GND	GND
P19	GBE_MDI3-	GBE0_MDI3-
P20	GBE_MDI3+	GBE0_MDI3+
P21	GBE_LINK100#	GBE0_LINK100#
P22	GBE_LINK1000#	GBE0_LINK1000#
P23	GBE_MDI2-	GBE0_MDI2-
P24	GBE_MDI2+	GBE0_MDI2+
P25	GBE_LINK_ACT#	GBE0_LINK_ACT#
P26	GBE_MDI1-	GBE0_MDI1-
P27	GBE_MDI1+	GBE0_MDI1+
P28	GBE_CTREF	GBE0_CTREF
P29	GBE_MDI0-	GBE0_MDI0-
P30	GBE_MDI0+	GBE0_MDI0+
P31	SPI0_CS1#	SPI0_CS1#
P32	GND	GND
P33	SDIO_WP	SDIO_WP
P34	SDIO_CMD	SDIO_CMD
P35	SDIO_CD#	SDIO_CD#
P36	SDIO_CK	SDIO_CK
P37	SDIO_PWR_EN	SDIO_PWR_EN
P38	GND	GND
P39	SDIO_D0	SDIO_D0
P40	SDIO_D1	SDIO_D1
P41	SDIO_D2	SDIO_D2
P42	SDIO_D3	SDIO_D3
P43	SPI0_CS0#	SPI0_CS0#
P44	SPI0_CK	SPI0_CK

Pin	SMARC 1.1	SMARC 2.0
P45	SPI0_DIN	SPI0_DIN
P46	SPI0_DO	SPI0_DO
P47	GND	GND
P48	SATA_TX+	SATA_TX+
P49	SATA_TX-	SATA_TX-
P50	GND	GND
P51	SATA_RX+	SATA_RX+
P52	SATA_RX-	SATA_RX-
P53	GND	GND
P54	~~SPI1_CS0#~~	ESPI_CS0#
P55	~~SPI1_CS1#~~	ESPI_CS1#
P56	~~SPI1_CK~~	ESPI_CK
P57	~~SPI1_DIN~~	ESPI_IO_0
P58	~~SPI1_DO~~	ESPI_IO_1
P59	GND	GND
P60	USB0+	USB0+
P61	USB0-	USB0-
P62	USB0_EN_OC#	USB0_EN_OC#
P63	USB0_VBUS_DET	USB0_VBUS_DET
P64	USB0_OTG_ID	USB0_OTG_ID
P65	USB1+	USB1+
P66	USB1-	USB1-
P67	USB1_EN_OC#	USB1_EN_OC#
P68	GND	GND
P69	USB2+	USB2+
P70	USB2-	USB2-
P71	USB2_EN_OC#	USB2_EN_OC#
P72	~~PCIE_C_PRSNT#~~	RSVD
P73	~~PCIE_B_PRSNT#~~	RSVD
P74	~~PCIE_A_PRSNT#~~	USB3_EN_OC#
P75	PCIE_A_RST#	PCIE_A_RST#
P76	~~PCIE_C_CKREQ#~~	USB4_EN_OC#
P77	~~PCIE_B_CKREQ#~~	RSVD
P78	~~PCIE_A_CKREQ#~~	RSVD
P79	GND	GND
P80	PCIE_C_REFCK+	PCIE_C_REFCK+
P81	PCIE_C_REFCK-	PCIE_C_REFCK-
P82	GND	GND
P83	PCIE_A_REFCK+	PCIE_A_REFCK+
P84	PCIE_A_REFCK-	PCIE_A_REFCK-
P85	GND	GND
P86	PCIE_A_RX+	PCIE_A_RX+
P87	PCIE_A_RX-	PCIE_A_RX-
P88	GND	GND
P89	PCIE_A_TX+	PCIE_A_TX+
P90	PCIE_A_TX-	PCIE_A_TX-

Pin	SMARC 1.1	SMARC 2.0
P91	GND	GND
P92	HDMI_D2+	HDMI_D2+ / DP1_LANE0+
P93	HDMI_D2-	HDMI_D2- / DP1_LANE0-
P94	GND	GND
P95	HDMI_D1+	HDMI_D1+ / DP1_LANE1+
P96	HDMI_D1-	HDMI_D1- / DP1_LANE1-
P97	GND	GND
P98	HDMI_D0+	HDMI_D0+ / DP1_LANE2+
P99	HDMI_D0-	HDMI_D0- / DP1_LANE2-
P100	GND	GND
P101	HDMI_CK+	HDMI_CK+ / DP1_LANE3+
P102	HDMI_CK-	HDMI_CK- / DP1_LANE3-
P103	GND	GND
P104	HDMI_HPD	HDMI_HPD / DP1_HPD
P105	HDMI_CTRL_CK	HDMI_CTRL_CK / DP1_AUX+
P106	HDMI_CTRL_DAT	HDMI_CTRL_DAT / DP1_AUX-
P107	~~HDMI_CEC~~	DP1_AUX_SEL
P108	GPIO0 / CAM0_PWR#	GPIO0 / CAM0_PWR#
P109	GPIO1 / CAM1_PWR#	GPIO1 / CAM1_PWR#
P110	GPIO2 / CAM0_RST#	GPIO2 / CAM0_RST#
P111	GPIO3 / CAM1_RST#	GPIO3 / CAM1_RST#
P112	GPIO4 / HDA_RST#	GPIO4 / HDA_RST#
P113	GPIO5 / PWM_OUT	GPIO5 / PWM_OUT
P114	GPIO6 / TACHIN	GPIO6 / TACHIN
P115	GPIO7 ~~/ PCAM_FLD~~	GPIO7
P116	GPIO8 ~~/ CAN0_ERR#~~	GPIO8
P117	GPIO9 ~~/ CAN1_ERR#~~	GPIO9
P118	GPIO10	GPIO10
P119	GPIO11	GPIO11
P120	GND	GND
P121	I2C_PM_CK	I2C_PM_CK
P122	I2C_PM_DAT	I2C_PM_DAT
P123	BOOT_SEL0#	BOOT_SEL0#
P124	BOOT_SEL1#	BOOT_SEL1#
P125	BOOT_SEL2#	BOOT_SEL2#
P126	RESET_OUT#	RESET_OUT#
P127	RESET_IN#	RESET_IN#
P128	POWER_BTN#	POWER_BTN#
P129	SER0_TX	SER0_TX
P130	SER0_RX	SER0_RX
P131	SER0_RTS#	SER0_RTS#
P132	SER0_CTS#	SER0_CTS#
P133	GND	GND
P134	SER1_TX	SER1_TX
P135	SER1_RX	SER1_RX
P136	SER2_TX	SER2_TX

Pin	SMARC 1.1	SMARC 2.0
P137	SER2_RX	SER2_RX
P138	SER2_RTS#	SER2_RTS#
P139	SER2_CTS#	SER2_CTS#
P140	SER3_TX	SER3_TX
P141	SER3_RX	SER3_RX
P142	GND	GND
P143	CAN0_TX	CAN0_TX
P144	CAN0_RX	CAN0_RX
P145	CAN1_TX	CAN1_TX
P146	CAN1_RX	CAN1_RX
P147	VDD_IN	VDD_IN
P148	VDD_IN	VDD_IN
P149	VDD_IN	VDD_IN
P150	VDD_IN	VDD_IN
P151	VDD_IN	VDD_IN
P152	VDD_IN	VDD_IN
P153	VDD_IN	VDD_IN
P154	VDD_IN	VDD_IN
P155	VDD_IN	VDD_IN
P156	VDD_IN	VDD_IN
S1	~~PCAM_VSYNC~~	CSI1_TX+ / I2C_CAM1_CK
S2	~~PCAM_HSYNC~~	CSI1_TX- / I2C_CAM1_DAT
S3	GND	GND
S4	~~PCAM_PXL_CK0~~	RSVD
S5	I2C_CAM_CK	CSI0_TX- / I2C_CAM0_CK
S6	CAM_MCK	CAM_MCK
S7	I2C_CAM_DAT	CSI0_TX+ / I2C_CAM0_DAT
S8	CSI0_CK+ ~~/ PCAM_D10~~	CSI0_CK+
S9	CSI0_CK- ~~/ PCAM_D11~~	CSI0_CK-
S10	GND	GND
S11	CSI0_D0+ ~~/ PCAM_D12~~	CSI0_RX0+
S12	CSI0_D0- ~~/ PCAM_D13~~	CSI0_RX0-
S13	GND	GND
S14	CSI0_D1+ ~~/ PCAM_D14~~	CSI0_RX1+
S15	CSI0_D1- ~~/ PCAM_D15~~	CSI0_RX1-
S16	GND	GND
S17	~~AFB0_OUT~~	GBE1_MDI0+
S18	~~AFB1_OUT~~	GBE1_MDI0-
S19	~~AFB2_OUT~~	GBE1_LINK100#
S20	~~AFB3_IN~~	GBE1_MDI1+
S21	~~AFB4_IN~~	GBE1_MDI1-
S22	~~AFB5_IN~~	GBE1_LINK1000#
S23	~~AFB6_PTIO~~	GBE1_MDI2+
S24	~~AFB7_PTIO~~	GBE1_MDI2-
S25	GND	GND
S26	~~SDMMC_D0~~	GBE1_MDI3+

Pin	SMARC 1.1	SMARC 2.0
S27	~~SDMMC_D1~~	GBE1_MDI3-
S28	~~SDMMC_D2~~	GBE1_CTREF
S29	~~SDMMC_D3~~	PCIE_D_TX+
S30	~~SDMMC_D4~~	PCIE_D_TX-
S31	~~SDMMC_D5~~	GBE1_LINK_ACT#
S32	~~SDMMC_D6~~	PCIE_D_RX+
S33	~~SDMMC_D7~~	PCIE_D_RX-
S34	GND	GND
S35	~~SDMMC_CK~~	USB4+
S36	~~SDMMC_CMD~~	USB4-
S37	~~SDMMC_RST#~~	USB3_VBUS_DET
S38	AUDIO_MCK	AUDIO_MCK
S39	I2S0_LRCK	I2S0_LRCK
S40	I2S0_SDOUT	I2S0_SDOUT
S41	I2S0_SDIN	I2S0_SDIN
S42	I2S0_CK	I2S0_CK
S43	~~I2S1_LRCK~~	ESPI_ALERT0#
S44	~~I2S1_SDOUT~~	ESPI_ALERT1#
S45	~~I2S1_SDIN~~	RSVD
S46	~~I2S1_CK~~	RSVD
S47	GND	GND
S48	I2C_GP_CK	I2C_GP_CK
S49	I2C_GP_DAT	I2C_GP_DAT
S50	I2S2_LRCK	HDA_SYNC / I2S2_LRCK
S51	I2S2_SDOUT	HDA_SDO / I2S2_SDOUT
S52	I2S2_SDIN	HDA_SDI / I2S2_SDIN
S53	I2S2_CK	HDA_CK / I2S2_CK
S54	SATA_ACT#	SATA_ACT#
S55	~~AFB8_PTIO~~	USB5_EN_OC#
S56	~~AFB9_PTIO~~	ESPI_IO_2
S57	~~PCAM_ON_CSI0#~~	ESPI_IO_3
S58	~~PCAM_ON_CSI1#~~	ESPI_RESET#
S59	~~SPDIF_OUT~~	USB5+
S60	~~SPDIF_IN~~	USB5-
S61	GND	GND
S62	~~AFB_DIFF0+~~	USB3_SSTX+
S63	~~AFB_DIFF0-~~	USB3_SSTX-
S64	GND	GND
S65	~~AFB_DIFF1+~~	USB3_SSRX+
S66	~~AFB_DIFF1-~~	USB3_SSRX-
S67	GND	GND
S68	~~AFB_DIFF2+~~	USB3+
S69	~~AFB_DIFF2-~~	USB3-
S70	GND	GND
S71	~~AFB_DIFF3+~~	USB2_SSTX+
S72	~~AFB_DIFF3-~~	USB2_SSTX-

Pin	SMARC 1.1	SMARC 2.0
S73	GND	GND
S74	~~AFB_DIFF4+~~	USB2_SSRX+
S75	~~AFB_DIFF4-~~	USB2_SSRX-
S76	PCIE_B_RST#	PCIE_B_RST#
S77	PCIE_C_RST#	PCIE_C_RST#
S78	PCIE_C_RX+	PCIE_C_RX+
S79	PCIE_C_RX-	PCIE_C_RX-
S80	GND	GND
S81	PCIE_C_TX+	PCIE_C_TX+
S82	PCIE_C_TX-	PCIE_C_TX-
S83	GND	GND
S84	PCIE_B_REFCK+	PCIE_B_REFCK+
S85	PCIE_B_REFCK-	PCIE_B_REFCK-
S86	GND	GND
S87	PCIE_B_RX+	PCIE_B_RX+
S88	PCIE_B_RX-	PCIE_B_RX-
S89	GND	GND
S90	PCIE_B_TX+	PCIE_B_TX+
S91	PCIE_B_TX-	PCIE_B_TX-
S92	GND	GND
S93	~~LCD_D0~~	DP0_LANE0+
S94	~~LCD_D1~~	DP0_LANE0-
S95	~~LCD_D2~~	DP0_AUX_SEL
S96	~~LCD_D3~~	DP0_LANE1+
S97	~~LCD_D4~~	DP0_LANE1-
S98	~~LCD_D5~~	DP0_HPD
S99	~~LCD_D6~~	DP0_LANE2+
S100	~~LCD_D7~~	DP0_LANE2-
S101	GND	GND
S102	~~LCD_D8~~	DP0_LANE3+
S103	~~LCD_D9~~	DP0_LANE3-
S104	~~LCD_D10~~	USB3_OTG_ID
S105	~~LCD_D11~~	DP0_AUX+
S106	~~LCD_D12~~	DP0_AUX-
S107	~~LCD_D13~~	LCD1_BKLT_EN
S108	~~LCD_D14~~	LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+
S109	~~LCD_D15~~	LVDS1_CK- / eDP1_AUX- / DSI1_CLK-
S110	GND	GND
S111	~~LCD_D16~~	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+
S112	~~LCD_D17~~	LVDS1_0- / eDP1_TX0- / DSI1_D0-
S113	~~LCD_D18~~	eDP1_HPD
S114	~~LCD_D19~~	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+
S115	~~LCD_D20~~	LVDS1_1- / eDP1_TX1- / DSI1_D1-
S116	~~LCD_D21~~	LCD1_VDD_EN
S117	~~LCD_D22~~	LVDS1_2+ / eDP1_TX2+ / DSI1_D2+
S118	~~LCD_D23~~	LVDS1_2- / eDP1_TX2- / DSI1_D2-

Pin	SMARC 1.1	SMARC 2.0
S119	GND	GND
S120	~~LCD_DE~~	LVDS1_3+ / eDP1_TX3+ / DSI1_D3+
S121	~~LCD_VS~~	LVDS1_3- / eDP1_TX3- / DSI1_D3-
S122	~~LCD_HS~~	LCD1_BKLT_PWM
S123	~~LCD_PCK~~	RSVD
S124	GND	GND
S125	LVDS0+	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+
S126	LVDS0-	LVDS0_0- / eDP0_TX0- / DSI0_D0-
S127	LCD_BKLT_EN	LCD0_BKLT_EN
S128	LVDS1+	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+
S129	LVDS1-	LVDS0_1- / eDP0_TX1- / DSI0_D1-
S130	GND	GND
S131	LVDS2+	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+
S132	LVDS2-	LVDS0_2- / eDP0_TX2- / DSI0_D2-
S133	LCD_VDD_EN	LCD0_VDD_EN
S134	LVDS_CK+	LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+
S135	LVDS_CK-	LVDS0_CK- / eDP0_AUX- / DSI0_CLK-
S136	GND	GND
S137	LVDS3+	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+
S138	LVDS3-	LVDS0_3- / eDP0_TX3- / DSI0_D3-
S139	I2C_LCD_CK	I2C_LCD_CK
S140	I2C_LCD_DAT	I2C_LCD_DAT
S141	LCD_BKLT_PWM	LCD0_BKLT_PWM
S142	RSVD	RSVD
S143	GND	GND
S144	~~RSVD /~~ EDP_HPD	eDP0_HPD
S145	WDT_TIME_OUT#	WDT_TIME_OUT#
S146	PCIE_WAKE#	PCIE_WAKE#
S147	VDD_RTC	VDD_RTC
S148	LID#	LID#
S149	SLEEP#	SLEEP#
S150	VIN_PWR_BAD#	VIN_PWR_BAD#
S151	CHARGING#	CHARGING#
S152	CHARGER_PRSNT#	CHARGER_PRSNT#
S153	CARRIER_STBY#	CARRIER_STBY#
S154	CARRIER_PWR_ON	CARRIER_PWR_ON
S155	FORCE_RECOV#	FORCE_RECOV#
S156	BATLOW#	BATLOW#
S157	TEST#	TEST#
S158	GND	GND